TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

MAXIM HIRVIMÄKI

COMPONENT TESTING FOR SPACECRAFT POWER SUBSYSTEM PASSIVATION FUNCTION

Master of Science Thesis

Examiner: Professor Karri Palovuori
Examiner and topic approved by the Faculty Council of the Faculty of Computing and Electrical Engineering on 31st of May in 2017.

PREFACE

I would like to thank RUAG Space Finland for providing the thesis topic, access to the previous research on passivation in order to write the theory part of this thesis and providing funding while the thesis contract lasted. I would additionally like to thank Juha Kuitunen and Juhani Simola from RUAG Space Finland for help regarding the thesis. I would like to thank Professor Karri Palovuori for being an examiner for this thesis and providing the necessary feedback. I would also like to thank Tampere University of Technology department of Electronics and Communications for funding most of the equipment of the miniature test system. Additionally I would like to thank staff of TUTLab for helping me with the manufacture of the miniature test system. The work for the test plan part of this thesis was done on RUAG Space Finland's premises using RUAG Space Finland's equipment from June of 2017 to February of 2018. The schematics and layouts for the semiconductor portion of the full test system prototype and plans, production and manufacture of the miniature test system of this thesis were done on Tampere University of Technology premises. Equipment and CAD software in Electronics and Communications department and TUTLab was used in the creation of the miniature test system and the layout and schematic design of the full-scale semiconductor test system.

ABSTRACT

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The amount of space debris has been increasing since the beginning of the space age. Unmanned spacecraft has energy storing components on-board which may pose a risk of causing the fragmentation of the spacecraft after the end of satellite lifetime. In order to mitigate aforementioned risks the spacecraft must be passivated at the end of its mission. In this thesis rationale to perform passivation is presented and several example methods to achieve passivation are listed and defined. Components with which the passivation can be achieved are introduced, detailed and compared. Due to long life-time data being unknown for relays and semiconductors temperature based test parameters are proposed to the aforementioned components. Additionally due to unknown high-voltage behaviour of bypass switches, parameters for switching test are proposed. A detailed test setup for semiconductor portion of testable components was created. A miniature test setup prototype based on the full-scale semiconductor test setup was built and a low number of commercial grade diodes and MOSFETs were tested using the built setup. In order to evaluate the possibility of the parameter measurements using the designed and built setup, the measured results were compared to the values present in the datasheets of the tested components.

TIIVISTELMÄ

MAXIM HIRVIMÄKI: Avaruusaluksen tehoalijärjestelmän passivointifunktion komponenttien testaus
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Avainsanat: passivointi, avaruusalus, satelliitti, PCDU, avaruusromun vähentäminen, testiasetelma, elämäkertatesti, lämpösyklinen testi

Avaruusromun määrä on lisääntynyt avaruusajan alusta asti. Miehittämättömissä avaruusaluksissa on kyydissä energiaa varastoivia komponentteja, jotka voivat aiheuttaa satelliitin sirpaloitumisriskin satelliitin elämänkerran lopun jälkeen. Sirpaloitumisriskin vähentämiseksi avaruusalukset tulee passivoida niiden missioiden loputtua. Työssä esitellään syitä passivoinnille sekä määritellään esimerkkejä passivointitavoista. Passivointiin käytettäviä komponentteja myös esitellään ja vertaillaan. Releiden ja puolijohteiden pitkäaikaisen käyttäytymistiedon puutteesta johtuen kyseisille komponenteille esitetään lämpötilaikäännyttämistestiparametreja. Ohituskytkimille esitetään myös kytkemistestin parametrit komponenttityypin suurjännitekäyttäytymistiedon puutteen takia. Puolijohteille määritellään myös yksityiskohtainen testijärjestelmä. Yksityiskohtaisesta puolijohteiden testijärjestelmästä tehdyn pienoisversion prototyypin toteutus esitellään työssä ja kyseisen järjestelmän avulla testataan pieniä määriä kuluttajatason MOSFETeja ja diodeja. Rakennetun testijärjestelmän soveltuvuutta arvioidaan mittaamalla testissä olevien komponenttien parametreja ja vertaamalla mittaustuloksia datalehtien arvoihin.

TABLE OF CONTENTS

TABLE OF TABLES

TABLE OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

ESA	European Space Agency
ISO	International Organization for Standardization
LEO	Low Earth Orbit
GEO	Geostationary Orbit
EPS	Electrical Power Subsystem
PCDU	Power Control and Distribution Unit
OBC	On-board Computer
MLI	Multi-layer Insulation
MB	Main Bus
PTC	Positive Temperature Coefficient
CID	Current Interruption Device
SBS	Simple Balancing System
EoC	End of Charge
RIU	Remote Interface Unit
MOSFET	Metal-oxide -semiconductor Field-effect Transistor
SA	Solar Array
SADM	Solar Array Drive Mechanism
SAPU	Solar Array Passivation Unit
PCB	Printed Circuit Board
Ref-Des	Reference Designator
CAD	Computer Aided Design

1 INTRODUCTION

Space debris is comprised of all man-made objects, including elements and fragments of the aforementioned objects, which are non-functional and are located in Earth orbit or are re-entering Earth's atmosphere [1]. The amount of space debris has been increasing since the launch of the Sputnik 1 in 4.10.1957. A summary of space debris and numbers on its quantities made by European Space Agency (ESA) can be found in Table 1.1.

Table 1.1 Space debris in January 2017 [2]

Description	Quantity
Objects with diameter from 1 mm to 1 cm	166 000 000
Objects with diameter from 1 cm to 10 cm	750 000
Objects with diameter larger than 10 cm	29 000
Total mass of objects in Earth orbit	about 7500 tonnes

In order to prevent further space debris, mitigation actions need to be taken. Several national and international agencies have adopted standards and proposed guidelines for space debris mitigation, the compendium of which was made by United Nations Office for Space Affairs [3]. All major European space agencies agreed on "European Code of Conduct for Space Debris Mitigation" in 2004 and first ESA Space Debris Policy was released in 2008. International Organization for Standardization (ISO) has released first edition of ISO24113 standard in 2010, which specifies the space debris mitigation requirements. The standard was updated in 2011 by a second edition [1]. European Committee for Space Standardization has released an adoption notice of the ISO24113:2011 standard in 2012 [4]. The policy of ESA has been updated in 2014 to use ECSS-U-AS-10C/ISO24113 standard [5]. It is stated in ISO24113:2011 section 6.2.2 in regards to preventing accidental break-ups of spacecraft:

"During the disposal phase, a spacecraft or launch vehicle shall permanently deplete or make safe all remaining on-board sources of stored energy in a controlled sequence." [1]

Electrical subsystem of a spacecraft contains sources of energy to which the cited statement applies. Electrical subsystem passivation is thus one of the methods to deplete or make safe the on-board sources of stored energy. The passivation mechanisms are initiated in a controlled manner when the spacecraft enters its disposal phase.

First four parts of this thesis consist of background information on passivation based mainly on studies conducted by RUAG Space Finland. Spacecraft passivation -chapter explains the reasons for passivation, lists some recommendations regarding passivation methods and presents considerations for battery safety. Passivation function chapter of the thesis lists several methods of passivation grouped into subcategories based on the structure of spacecraft and its power subsystem. Components in passivation chapter lists possible main components to be used in spacecraft passivation and explains the operation of the component types. The fifth chapter proposes the tests for the passivation components and provides a design for a test setup for the semiconductor portion of the components. In sixth chapter an implementation of a miniature version of the designed semiconductor test setup is reviewed.

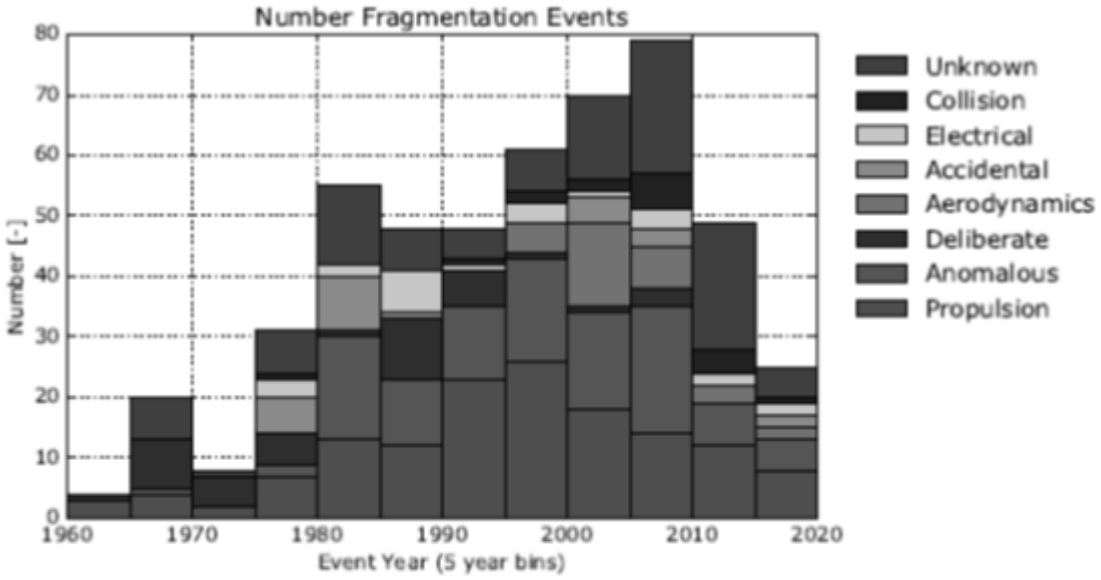
2 SPACECRAFT PASSIVATION

Space debris poses a significant risk of collision with operational spacecraft, which may be destroyed or damaged in the event of impact. Space debris' re-entry of Earth's atmosphere can also pose a hazard to human population, air and naval traffic, ground and sea assets in case the mass of the debris or its fragments is enough to reach Earth's surface with high kinetic energy. According to ESA's Annual Space Environment Report there are 18485 catalogued objects orbiting the Earth in 2016 [6]. According to the report, the number of re-entered objects was 235 in the same year. It is mentioned in the ESA Space Debris Mitigation Compliance Verification Guidelines, that typically from 10% to 40% of the mass of a re-entered object can survive the re-entry into Earths atmosphere [7].

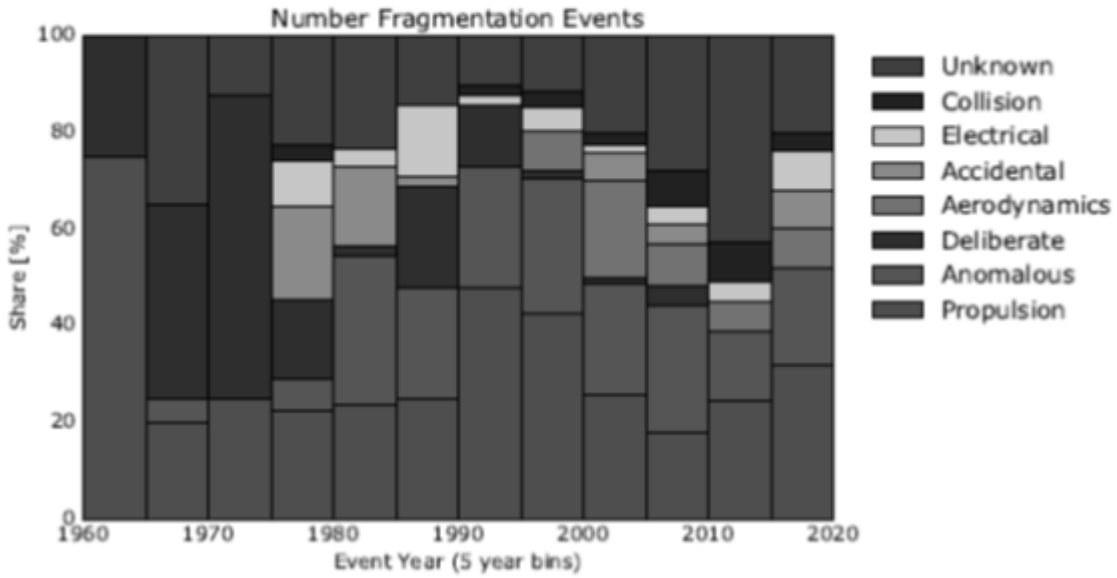
This section of thesis provides a general overview of passivation of a spacecraft. In the first part, the reasons for spacecraft passivation are listed and explained. In the second part, the recommendations for a general overview are given on the passivation functions. Due to the thesis focusing on the electrical passivation of the power subsystem of a spacecraft, the safety recommendations for power subsystem are listed in the third part of this chapter. The topics overviewed in this section are summarized in the fourth and last part.

2.1 Passivation Rationale

The breakup of launch vehicles or spacecraft can contribute to space debris. According to ESA's Annual Space Environment Report there have been 480 confirmed fragmentation events (spacecraft breaking up into fragments) since the beginning of space age until January 2017 [2].The chart in ESA's Annual Space Environment Report, which subcategorizes the fragmentation events by causes, is illustrated in Figure 2.1.



(a) Absolute number of fragmentation events per event cause.



(b) Relative number of fragmentation events per event cause.

Figure 2.1 Number of fragmentation events from 1960 to January 2017 [2]

"*Electrical"* fragmentation cause in Figure 2.1 is described in the Environment Report as the following:

"Most of the events in this category occurred due to an overcharging and subsequent explosion of batteries. A sub-class is defined based on the satellite bus." [2]

ESA has released Space Debris Mitigation Compliance Verification Guidelines in order for the missions of the agency to comply with the ECSS-U-AS-10C/ISO24113 standard [7]. The rationale for passivation provided by the guidelines is to prevent the spacecraft from accidentally breaking up after the operational phase of the mission and the disposal

phase by making safe or depleting all the on-board sources of energy just as stated in ISO24113 standard. Examples leading up to spacecraft break up events in regards to electrical systems given by the guidelines are the following in section 4.11.1b:

"Explosions or bursts of battery cells, which can result, for example, from cell degradation, exothermal chemical reactions, short-circuit, overcharge, overdischarge, overpressure, corrosion, and Stress Corrosion Cracking (SCC)."
[7]

In order to make the designed spacecraft to comply with the passivation requirement of making safe or depleting the stored energy, the mitigation guideline handbook provides four methods in section 4.11.2 [7]. First method is to identify all the components, which have to possibility to store residual energy or need to be depleted before the spacecraft disposal. Second method is to describe the implemented measures for making safe or depleting the component considering the passivation environment. In case of the components being unable to be fully depleted, the rationale for the acceptance of use of such components needs to be provided according to the third method. According to last method, the dynamic simulations of the operations of the spacecraft not resulting in an unpredictable altitude or orbit need to be provided.

2.2 Recommendations and Considerations

In a passivation study performed on Airbus DS Low-Earth-Orbit (LEO) power control and distribution units (PCDU) are listed several recommendations for passivation on which this chapter is based upon [8]. According to the study, the activation of passivation must be one failure tolerant regarding its unintentional activation in terms of both passivation control electronics and the power components. To pass the one failure tolerance requirement the device has to be able to endure a single failure in the aforementioned areas. If more than a single failure occurs in both the passivation control electronics and the power component, the device is not expected to be able to operate normally. The one failure tolerance requirement however is not applicable to electronics of the passivation device [8].

In the Airbus DS LEO PCDU study it is recommended that the passivation must be in some cases reversible by design at least until the On-Board-Computer (OBC) of the spacecraft is no longer operable and/or the energy sources are no longer available [8]. Typically for satellites on Low-Earth-Orbit operational phase lasts for 15 years and disposal phase lasts for 25 years. Passivation device must thus be able to operate for at least the 25 years in orbit after passivation during which the thermal control is no longer available resulting in extreme temperature conditions, which are in excess of operational

temperatures for some electronic and electromechanical components and/or associated state of the art manufacturing processes [8].

In a study made by ESA important aspects in regards of passivation are listed [9]. The list compiles the considerations detailed in a technical document [10]. According to the list the factors that need to be accounted for in the design of passivation function are loss of thermal control after passivation, possible effects of radiation, life time of the passivation device, reliability of the passivation device before and after passivation, number of safety barriers in order to avoid premature passivation, safe discharge and state of charge, the autonomy level of the passivation function, operations including observability and duration of passivation process, testability of the passivation, mandatory steps to achieve space qualification, costs and considerations in regards to competiveness and the possibility to standardize the concept. Some of these considerations are applied in the comparison between the components used in passivation in chapter 4.

2.3 Battery Safety

Satellite battery serves as the main power source throughout the lifetime of the spacecraft. The battery is also most dangerous of the components in the Electrical Power Subsystem (EPS) of the satellite due to possibility of the battery breaking up and creating fragments, which would contribute to space debris. The major abuse conditions that cause safety issues with lithium-ion batteries are the results of overcharge, short circuits, overdischarge, high temperature condition and structural issues [11]. The aforementioned events can cause the battery to enter thermal runaway and explode. Passivation devices aim to prevent the battery from breaking up during the disposal phase of the satellite. In addition to the passivation devices, some battery types have additional protection mechanisms, some of which are introduced in this chapter in addition to the possible battery types used in the satellites.

RUAG Space Finland with partnership Airbus DS and informative inputs from SAFT and ABSL performed an assessment of battery safety for ESA on batteries comprised of the following cell types: ABSL 18650 HC, 18650 NL small capacity cell, SAFT VES16 small capacity cell and SAFT VES180 high capacity cell [12]. In the batteries selected for battery safety assessment the following battery cell internal safety protections were incorporated in the ABSL 18650 cells: Positive Temperature Coefficient (PTC) poly-switch, shut down separator, Current Interruption Device (CID) and venting using the pressure disk. SAFT VES16 cells incorporate shut down separator, CID, pressure disk for venting and “leak before burst” -design as the internal safety measures of the cells. In addition to the aforementioned mechanisms, it is possible for batteries to have internal control electronics in order to balance the cells and increase the safety. SAFT VES180 only incorporates “leak before burst” –design as its internal safety mechanism.

In ABSL 18650HC cells the PTC poly-switch is implemented using semi-crystalline polymer impregnated with conductive particles [13]. In the event of high discharge current, the PTC is heated causing an expansion of the polymer due to the crystalline base melting [13]. The expansion of the polymer separates the conductive particles causing an increase in resistance and reduction of the current. The PTC poly-switch can be reset after it is sufficiently cooled down but the performance is degraded after activation [10].

Shut down separator is implemented in the batteries that were used in the safety assessment by utilizing a microporous polyethylene separator on the cathode and anode of the battery cells [10]. In the event where the cell temperature would exceed certain defined safety parameters, one of the three polyethylene layers in the shutdown separator would melt and cut the ion flow [10]. The cut of ion flow would result the cell being in open circuit failure mode.

CID operation is based on pressure conditions of the battery cells and is implemented using a pressure disk. Due to decomposition of lithium carbonate gasses, the pressure is increased [13]. The disk separates from the conducting lead after reaching sufficient pressure resulting in stopping of the current flow. If the internal pressure is increased despite the CID activating, the pressure disk would vent the pressure. If the pressure would continue to increase despite the venting, the disk would burst. “Leak before burst” design strategy for battery cell casings based on allowing the casings to leak before bursting in order to prevent fragmentation. CAD (Computer Aided Design) representation of Sony 18650HC, which incorporates most of the internal safety mechanisms depicted in this paragraph, is presented in Figure 2.2. The operation of the pressure disk in ABSL 18650 cells is illustrated in Figure 2.3.

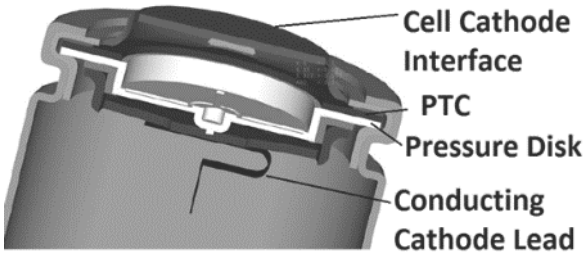


Figure 2.2 CAD representation of a Sony 18650 cell [11]

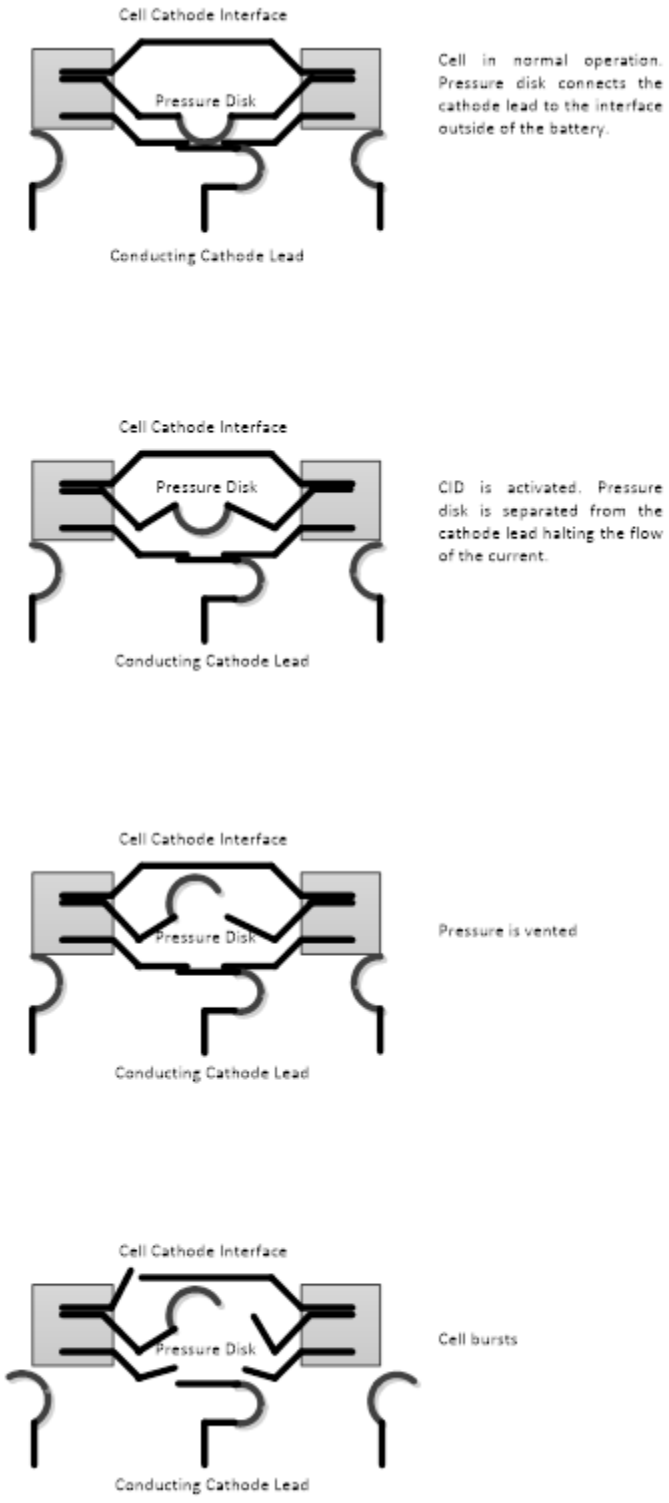


Figure 2.3 Simplified diagram of pressure disk operation in ABSL 18650 HC cells

The drawback unique to the lithium-ion battery technology is linked to the lack of ability to overcharge the lower energy cells of the battery when attempting to fully charge the cells with high voltage [14]. Overcharge leads to generating Li-ion plating on the negative electrode, which in turn leads to premature aging or thermal runaway with no threshold [14]. E. Mosset listed three main origins of cell voltage spread in batteries as

heterogeneous cell leakage current, heterogeneous cell electromechanical materials and heterogeneous cell temperatures [14]. ABSL battery detailed in the safety assessment done by RUAG Space Finland did not incorporate any internal control electronics nor was there a requirement for external control electronics [11]. Balancing of the ABSL battery is achieved by matched cell selection during a screening process during the manufacturing process [11]. VES16 possesses an autonomous simple balancing system (SBS) which is implemented across each battery cell [15]. VES180 batteries require external balancing system. One such system can be implemented in the power control and distribution unit on the satellite as was done in GALILEO satellites [16].

Despite batteries possessing several safety mechanisms, it is possible for the speed of thermal runaway to be too high for the protections to react [17]. Thus it is recommended that the battery meets the following conditions before entering the disposal phase of the satellite life based according to a passivation study [17]:

- The battery should be discharged to 50% state of charge or less
- The battery should avoid temperatures higher than 100 ◦C,
- The recharge of battery should be prevented after the beginning of passivation in order to avoid overcharging
- Cumulated radiation should not exceed defined values in case of the Li-ion cells themselves in addition to passivation electronics
- Passivation device shall be able to sustain the harsh environment after passivation to guarantee the battery safety

2.4 Summary

Breaking up of spacecraft creates fragments that contribute to space debris, which poses various threats in orbit or inside the Earth's atmosphere if the fragments retain enough mass after re-entry. Passivation of unmanned spacecraft is required in order to reduce the possibility of the break-up of the satellite.

When designing the passivation device several considerations need to be made. The passivation device is recommended to be reliable, have a long lifetime and able to endure extreme environmental conditions after the loss of the temperature control due to the satellite being in disposal phase.

Battery is the most dangerous component in the electrical power system of the satellite. Battery itself has several safety mechanisms on cell level or whole battery level, which are either autonomous or controlled by other devices. The safety mechanisms are not enough to passivate the spacecraft and thus several safety precautions need to be taken before entering the disposal phase regarding temperature conditions, radiation, battery charging and discharging in addition to state of charge of the battery needing to be as low as possible.

3 PASSIVATION FUNCTION

The Electrical Power Subsystem (EPS) of a satellite consists of a battery (the type of the battery is lithium-ion presently, but in the past nickel-cadmium batteries were used), solar array and a power control and distribution unit (PCDU). Main power for the satellite is distributed through the main bus (MB) and provided by the PCDU. The battery and solar array provide power to the PCDU, which in turn regulates the power to the main bus (MB) of the spacecraft and recharges the battery. The simplified block diagram of a typical satellite powering topology is illustrated in Figure 3.1.

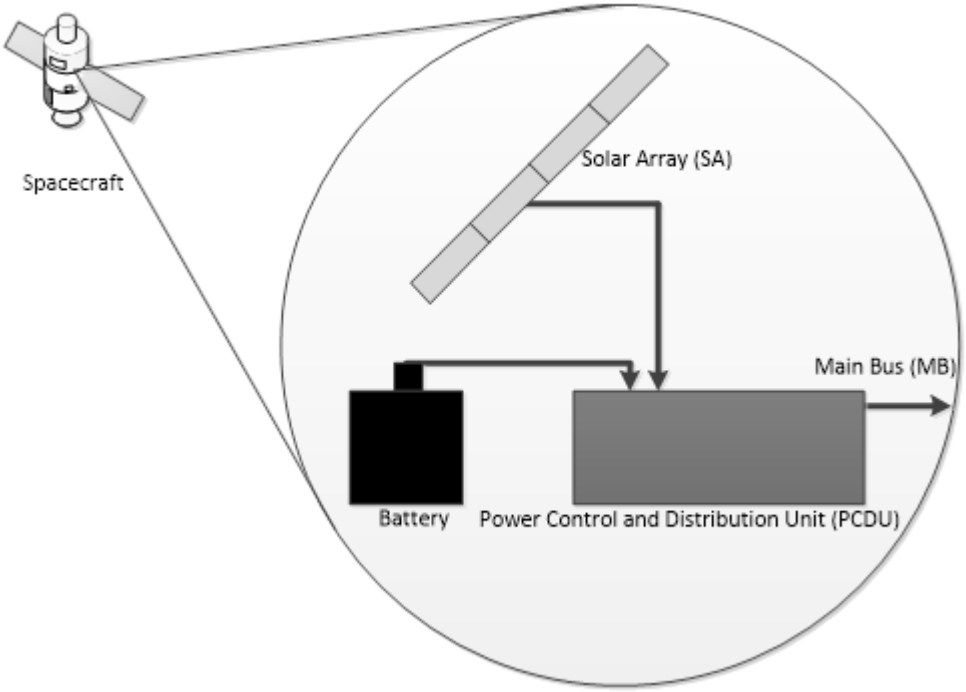


Figure 3.1 Block diagram of a satellite electrical power subsystem

The target of passivation is to ensure the safety of the EPS. In particular, the battery portion of the EPS is needed to be made safe due to the risk of the battery breaking down and creating space debris. European Space Agency Debris Mitigation Guidelines provides recommendations in regards to passivation measures for the power subsystem, which can be found in ANNEX E of the guidelines, and table based on the recommendations concerning the power subsystem is in Table 3.1 [7].

Table 3.1 Power subsystem passivation measures [7]

Component	Passivation Measures	Critical Issues and Remarks
Batteries	1. Self-protection 2. Discharge 3. Disconnection from charging sources 4. Depressurization of the battery cells(if needed)	- The discharge of batteries and their subsequent disconnection is the preferred method - Passivation device should be able to withstand the harsh environment after the satellite disposal in regards of loss of the temperature control and radiations from space - In the case the stored energy elimination and battery disconnection being impossible the self-protection of batteries can be triggered if the risk of breakup is absent and the absence of that risk is guaranteed - Small batteries can be protected in containers that would limit the debris propagation in case of explosion
Fuel Cells	1. Self-protection 2. Discharge 3. Disconnection from all the charging sources 4. Depressurization of the fuel cells (if needed)	- Same issues and remarks as in the case with batteries.
PCDU	1. Disconnection from power sources 2. Switching off all the possible circuits	- None provided in the guidelines.
SA	1. Disconnection from power bus or batteries 2. Short-circuit	- Same issues and remarks as in the case with batteries.

Even though fuel cells are part of the power subsystem of the spacecraft, they are not part of the electrical power subsystem and thus are not the focus of this thesis. In ESTEC workshop in 2013, several methods of passivation function implementation were proposed [19]. Study performed by RUAG Space Finland details several possibilities based on the proposed passivation functions in the ESTEC workshop presentation and the ESA Space Debris Mitigation Guidelines which are introduced in this chapter [20]. In this section of the thesis, potential passivation function implementations are grouped into four main categories based on the RUAG Space Finland's study.

3.1 Spacecraft Level

Battery placement, spacecraft movement and power management with the on-board computer can be used in passivation on spacecraft level. Spacecraft level passivation function cannot achieve passivation of the spacecraft on its own and is to be used be used together with other passivation methods.

One of the main conclusions of thermal assessment study done by Airbus DS [18] is that the placement of the battery heavily influences the temperature range that the battery is subjected to. To avoid sun flux that would heat up the battery it is recommended to place the battery inside the spacecraft. If the internal placement is not possible, it should be ensured that the multi-layer insulation (MLI), which acts as a protective layer for the satellite, is attached properly or reinforced to guarantee that the chance MLI being torn away before atmospheric re-entry is minimal. For satellites in LEO the risk of MLI being torn away is negligible [20]. For other orbits where the spacecraft is supposed to stay longer on the graveyard orbit, such as in the case the satellite is in geostationary orbit (GEO) orbit the risk of MLI tearing is more significant compared to LEO [20].

In the thermal analysis done by Airbus DS [18] it was concluded that the altitude of the spacecraft could also greatly affect the temperature range the battery is subjected to. Based on the same study it was concluded that if the spacecraft is spun at a certain rate before disposal, the maximum temperature the battery and the passivation device could be reduced, which in turn would reduce the risks of thermal runaway of the battery [20]. Before implementing the spinning of the spacecraft the possibility of the spacecraft to withstand the spinning should be confirmed. The spin rate would be progressively damped.

It is possible to aid the passivation function by using software [20]. The on-board computer (OBC) of the spacecraft could aid the passivation process by setting the spacecraft behavioural parameters in such a manner that the solar array would point away from the sun resulting in no power being provided to the satellite. PCDU would set the end of charge (EoC) current and voltage to the minimum values for the battery balancing system in order not to recharge the battery.

3.2 Battery Level

The proposed methods in ESA Space Debris Mitigation Compliance Verification Guidelines for spacecraft passivation on battery level to be usage of the battery self-protection, discharging of the battery, disconnection of the battery and depressurization of the battery cells as can be seen in Table 3.1. The solutions to aforementioned passivation methods have been reviewed and described in the passivation function implementation review done by RUAG Space Finland [20].

The implementation review proposes the usage of a dedicated battery charging and discharging circuit or an external load as the methods of the discharge of the battery [20]. External resistor network can be used an exertional load for example. The connection of the external load to the battery can be implemented using relays or battery bypass switches. A simplified example of battery discharging passivation function by an external load using a relay switch is illustrated in Figure 3.2.

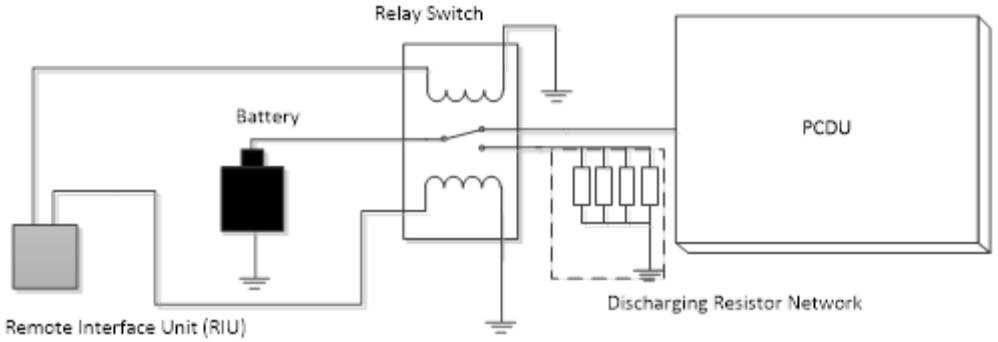


Figure 3.2 Battery disconnection and discharge using an external relay switch

In the implementation proposed in the Figure 3.2, the passivation is activated by a signal from the Remote Interface Unit (RIU) which would force the relay to switch battery to the external load in the form of discharging resistors. After the relay has switched the battery would become disconnected from PCDU and would provide no power to the system. The use of the external load reduces the required contact current rating of the used relay, which would possibly reduce the costs of the implementation due to the possible increase of relay variety that could be used. The resistor additionally discharges the battery depleting the battery cells.

The battery disconnection methods are proposed to be implemented using the battery internal protections or the internal or external switch of the PCDU [20]. While theoretically possible, a safe and practical way to activate battery internal protections in abnormal conditions was not found and therefore such battery disconnection method was not further considered in the RUAG Space Finland's study. The internal PCDU switch can be realized using MOSFETs or relays. A relay is used as an external switch and the implementation based on a relay is illustrated in Figure 3.2. The simplified internal MOSFET switch implementation is in Figure 3.3.

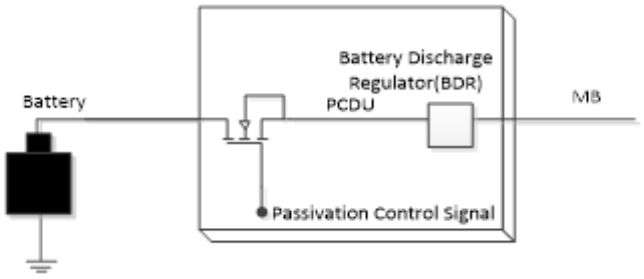


Figure 3.3 Battery disconnection using an internal MOSFET switch

In the internal switch implementation the battery would be disconnected once there is was passivation control signal, which would case the MOSFET to be in its cut-off state. Battery would be disconnected from the PCDU and would provide no power to the system. Due to the use of the internal components the cost and size of this implementation is small compared to other passivation functions discussed in this chapter.

In the passivation function implementation review by RUAG Space Finland the methods of short-circuiting the battery were studied [21]. The alternative methods to short-circuit the battery in the study were a battery bypass switch, battery balancing system and battery internal protections. Battery could be theoretically short-circuited using a battery bypass switch but the switch contact voltage is rated for individual battery cells several of which comprise a typical battery making the battery voltage exceed the rated contact voltage of the switch. One of the purposes of the component testing planned in this thesis was to find out bypass switch behaviour with higher contact voltage than the switch being initially designed for. Battery balancing systems are able to discharge the battery, but not prevent the recharge of the battery. No practical or safe way to use battery internal protections for short-circuiting the battery was found in the study. A simplified theoretical short-circuiting solution utilizing a bypass switch is illustrated in Figure 3.4

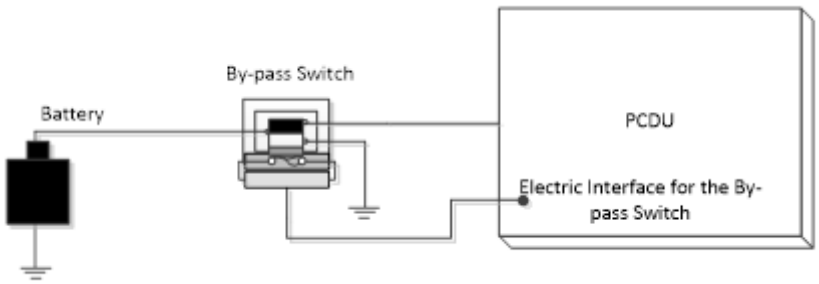


Figure 3.4 Short-circuiting of battery using a bypass switch.

Once activated, the bypass switch in Figure 3.4. would disconnect the battery from PCDU. Battery is disconnected from the charging circuitry of PCDU and is short-circuited once the bypass switch operation has been finalized.

3.3 Solar Array Level

ESA Space Debris Mitigation Compliance Verification Guidelines for spacecraft passivation lists short-circuiting or disconnection of the solar arrays as feasible methods for passivation of the spacecraft on the solar array level as can be seen in Table 3.1. This section of the thesis describing the passivation function on solar array level is based on the passivation function implementation methods studied by RUAG Space Finland in their implementation review [20].

The proposed methods to be used to disconnect the solar array in the implementation review were relays, cable cutters, MOSFETs or usage of solar array drive mechanisms (SADM). The simplified method of solar array disconnection utilizing a relay is in Figure 3.5. The simplified principle of SADM disconnection method is illustrated in Figure 3.6.

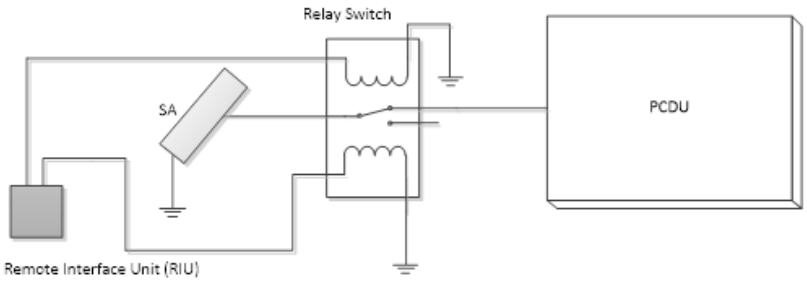


Figure 3.5 Solar array disconnection using a relay switch

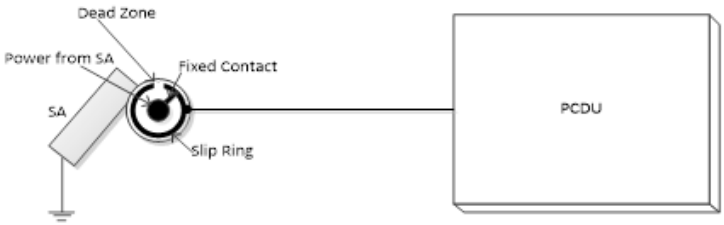


Figure 3.6 Solar array disconnection using a SADM slip ring

In Figure 3.5 the passivation would start by RIU receiving a signal and forcing the relay to switch which would disconnect the solar array from the PCDU. Disconnection using MOSFETs is similar to the method illustrated in Figure 3.3 with the battery in the figure replaced by a solar array. In the SADM implementation the slip ring would be rotated in such manner that the fixed contact is in dead zone during passivation, cutting the power from SA to the PCDU. In the passivation function implementation utilizing a cable-cutter the cable from the solar array to the PCDU is cut, disconnecting the solar array from the power subsystem.

Short-circuiting of solar array is proposed to be implemented using parallel MOSFETs, bypass switches, or a dedicated solar array passivation unit (SAPU). Simplified block diagram representing implementation utilizing parallel MOSFETs is illustrated in Figure

3.7. Simplified illustration of SAPU implementation is in Figure 3.8. The block diagram of short-circuiting of the solar array utilizing the bypass switch is similar compared to the short-circuiting of battery in Figure 3.4, with the battery replaced by a solar array in the figure.

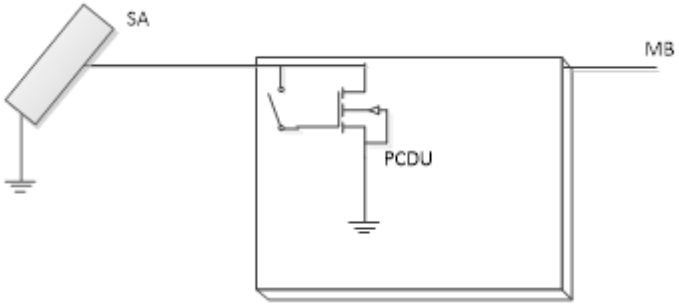


Figure 3.7 Solar array short-circuiting using a parallel MOSFET

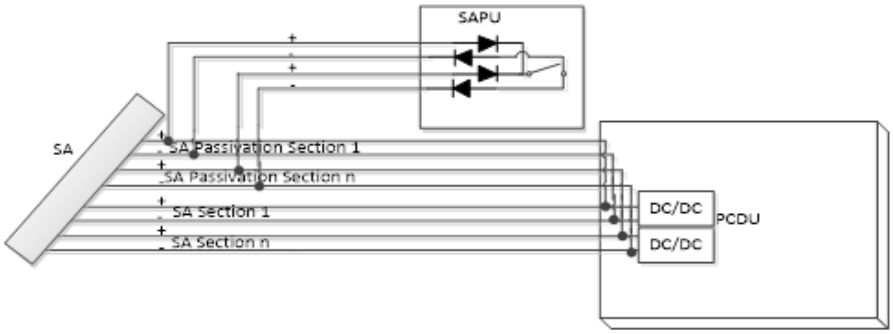


Figure 3.8 Solar array short-circuiting using SAPU

In the block diagram with MOSFET implementation in Figure 3.7 during passivation the gate of the transistor is connected to the solar array voltage causing the MOSFET to be in saturation or linear mode after the solar array voltage drops sufficiently low. Linear mode in MOSFETs would cause large power dissipation in comparison to saturation mode so this solution is not preferred. In the SAPU implementation of the passivation function illustrated in Figure 3.8 in which the poles of solar array sections are short-circuited with a switch and diodes. The switch in the SAPU implementation could be a relay for example.

3.4 Main Bus Level

In the passivation implementation review done by RUAG Space Finland it was concluded that passivation function could be performed on the main bus level by short-circuiting the bus [20]. The main bus short-circuit solution could be implemented using bypass switches or relays. Short-circuit solution using bypass switch is similar to the battery short-circuit implementation illustrated in Figure 3.4 with the battery replaced by the main bus. A simplified version of short-circuiting of the main bus using a relay is in Figure 3.9.

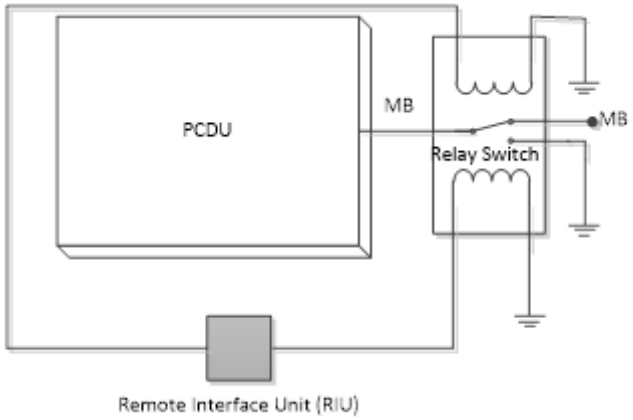


Figure 3.9 Short-circuiting the main bus using a relay

The operation of the passivation function illustrated in Figure 3.9 would begin by the RIU receiving the signal to energize the coil of the relay. Electromagnetic field would switch the relay in such way that the main bus would be connected to the ground resulting in a short-circuiting of the main bus.

3.5 Summary

Spacecraft passivation can be implemented on spacecraft level, battery level, solar array level and/or main bus level. Simplified summary of the methods examined in this chapter are illustrated in Figure 3.10. Due to the passivation function requiring the ability to endure single point failure the switches which would short circuit a part of the electric power subsystem are in series and the switches that would disconnect the system are in parallel. Failure of a single switching component would thus not cause accidental activation of the passivation function.

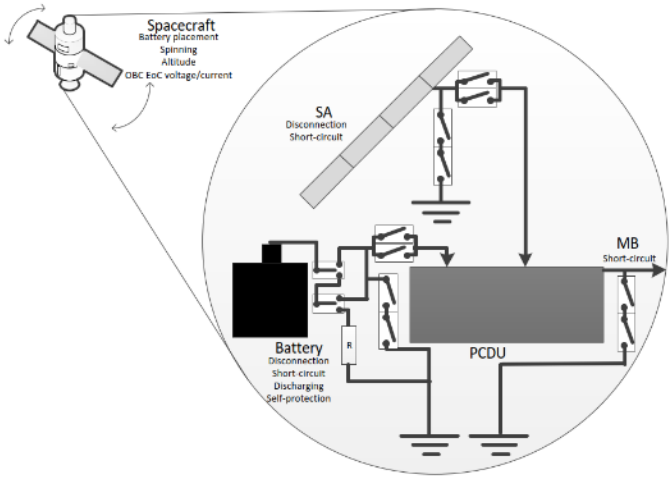


Figure 3.10 Summary of the examined passivation methods

Different electronic components can be used on different levels of the passivation function. The passivation function and the possible main components that shall be examined further in this thesis are listed in Table 3.2. Due to the single point failure

tolerance requirement there are at least two switches in each of the passivation functions in order to reduce the risk of accidental passivation function activation. In case the passivation is performed by short-circuiting the part of the subsystem the switches are in series. In the case the part of the subsystem is disconnected the switches are in parallel.

Table 3.2 Passivation function components relevant to the thesis in possible passivation functions

Level	**Passivation Function**	**Possible Components in thesis to use**
Battery	Disconnection	Relay, MOSFET, bypass switch
	Discharge	Relay with discharge resistors, bypass switch with discharge resistors
	Short-circuit	Bypass switch
Solar array	Disconnection	MOSFET, cable-cutter, relay
	Short-circuit	SAPU, relay, bypass switch
Main bus	Short-circuit	Relay, bypass switch

Other methods that theoretically could be used in passivation are battery self-protection, solar array drive mechanisms, software patch to set the charge voltage and currents to minimum, battery position in spacecraft and the movement of spacecraft. Battery disconnection, battery discharge, battery short-circuit, solar array disconnection and solar array short-circuit passivation functions were selected for the test of the components. According to passivation study performed on Airbus DS LEO PCDUs, in most of the requirement specifications the passivation methods are defined as battery disconnection, solar array disconnection and combination of battery and solar array disconnection [8].

4 COMPONENTS IN PASSIVATION FUNCTION

Several component types can be used in passivation function of the spacecraft. The components need to withstand harsh radiation and temperature levels in space in order to reduce the chance of battery thermal runaway after the thermal control of the system would be disabled. Due to the high standards and low number of manufacturers who can meet the standards the costs of the space qualified parts are around 100 times higher than commercial ones.

In this chapter, some of the components that can be used in the passivation function are introduced. The pros, cons and the usage and failure methods of the components are detailed. In addition to the components mentioned in this chapter, the use of internal safety mechanisms of the battery could theoretically be possible. There are no currently known safe or practical methods to activate the safety mechanisms however.

4.1 Relays

Relay is an electromechanical component which changes the state of its mechanical switch based on the magnetic field induced by the current flowing through the coil. The relays can be divided into latching and non-latching types. The latching type relay retains the position of the switch after the coil is de-energized and the switch position in the non-latching type relay resets after the coil is de-energized. Simplified operation principles for single-pole-double-throw (SPDT) and double-pole-double-throw (DPDT) type relay is illustrated in Figure 4.1.

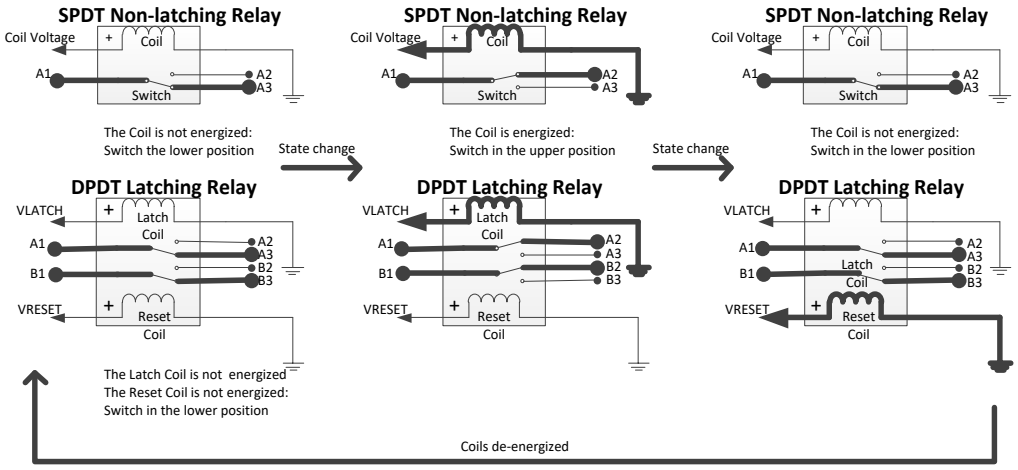


Figure 4.1 Operation of SPDT non-latching relay and DPDT latching relay current conducting paths are bolded

RUAG Space Finland performed a long-term behaviour analysis on components that could be used in passivation function and has defined several guidelines on relays in

regards to usability in the passivation function [21]. Due to no current being available to drive the relay the selection of latching type relay is recommended. If the relay is defined to be powerless during the passivation state the non-latching type relay could be used. However if the relay is non-latching, the coil of the relay must be energized the whole mission which may cause increase in power dissipation. To avoid relay contact state change the coils should be powered during the launch of the spacecraft.

When the coil of the relay is de-energized it induces reverse voltage which maintains current flow in the coil. The reverse voltage is inversely dependent on the duration of the de-energizing of the coil. Suppression circuits can be used to reduce the reverse voltage. The suppression circuits however decrease the contact reliability and may slow down the opening of contacts but due to passivation not being timing dependant and having very few switching action requirements (ideally the system is passivated only once) the negative effects of the suppression circuits are not relevant in regards to the passivation function.

Maximum switching voltage and minimum contact current limit the relay usability. Due to electromechanical nature the relay can be considered non sensitive for the radiation. The mechanics can only be degraded by very high radiation ratings, which are orbit and disposal duration dependent. The possible failure mechanisms and their probability as documented by the United States Department of Defence in electronics reliability handbook out of the failures are listed in Table 4.1 [22].

Table 4.1 Relay failure mechanisms [22]

Failure	**Probability**
Fails to trip	0.55
Spurious trip	0.26
Short	0.19

Several passivation configurations can be achieved using relays based on passivation function implementation review done by RUAG Space Finland [20]. Relays can be used in battery, solar array and main bus level. Relays can disconnect or aid to discharge the battery. The solar array can be disconnected or short-circuited using relays. The relays can also be used to short-circuit the main bus.

The favourable and unfavourable sides of using relays in the passivation function were listed by RUAG Space Finland [21]. The advantages of using the relays are that the relays are not radiation sensitive and are reliable compared to MOSFETs. The relays are easy to control and test and have low on-resistance and that there are already space qualified relays available. The cancellation of passivation function is also possible when using relays. The firing circuit of relays is pyro equivalent. The disadvantages of using relays

are that the power ratings of the contacts are limited compared to other components, the masses of relays are large compared to MOSFETs and that the coils of the relays could possibly cause magnetic momentum which could potentially affect the spacecraft position.

4.2 MOSFETs

MOSFETs are semiconductor devices, outputs of which are controlled by applying voltage to the gate terminal, which is isolated from the current conducting channel using silicone oxide. The applied voltage causes an electric field inside the transistor enhancing or depleting the p- or n-channel from the drain to the source terminals depending on the transistor type. MOSFET can be in three operation modes depending on voltages across its gate, source and drain terminals. The conditions to the operation modes can be expressed by the following equations in n-channel MOSFETs:

$$\textit{Cut-off mode: } V_{GS} < V_{Th}, \tag{1}$$

$$\textit{Triode or linear mode: } V_{GS} > V_{Th} \text{ AND } V_{DS} < (V_{GS} - V_{Th}), \tag{2}$$

$$\textit{Saturation mode: } V_{GS} > V_{Th} \text{ AND } V_{DS} \geq (V_{GS} - V_{Th}), \tag{3}$$

where V_{GS} is Gate-to-Source voltage, V_{Th} is threshold voltage and V_{DS} is Drain-to-Source voltage. In p-channel MOSFETs the conditions for the operation regions would be inverse of formulae 1, 2 and 3. In cut-off mode the Drain-to-Source current (I_{DS}) is small, but can still cause power dissipation. In linear mode I_{DS} is dependent on V_{DS} and V_{GS}. In saturation mode I_{DS} primarily depends on V_{GS}. If MOSFET is to be used as a switch such as in the passivation function, the transistor should be either in cut-off or saturation mode. MOSFET entering linear mode during passivation referred to as linear mode failure, which is an unwanted phenomenon that would increase the power dissipation.

Space qualified MOSFETs are usually packaged in TO-254, SMD-2, SMD-1 and SMD-0.5 packages. Due to the high currents going through the MOSFETs in passivation functions the potential used packages would be limited to TO-254, SMD-2 and SMD-1 [21]. The packages consist of several different materials with different thermal expansion factors. Due to the thermal expansion factors differing from material to material in the package, the package structure is affected by mechanical stress. In the long-term component behaviour analysis it is stated that the parts that are affected by the mechanical stresses are chips, dies, bonding wires, package materials and mounting base materials [21]. Failures caused by these mechanisms are that the device is open, short-circuited or in linear mode. Linear mode is considered the worst of the aforementioned failures due to the large power dissipation.

Semiconductors are sensitive to radiation mainly in forms of total ionizing dose (TID), single event effects (SEE) and displacement damage (DD) [23]. However MOSFETs do not typically suffer from effects of displacement damage [23]. Total ionizing dose (TID) accumulates during the life-time of the MOSFET and in case of p-channel MOSFETs may cause decrease in drive current and in the case of n-channel MOSFETs may change the threshold voltage [24]. Typical Radiation Hardened MOSFETs, which are could be used in space, have a radiation tolerance of 100 – 300 kRads (Si) with some types being able to endure radiation up to 1 000 kRads [21].

Out of single destructive event effects power metal-oxide semiconductors are summarized to be affected by single event burnouts (SEB) or single event gate ruptures (SEGR) in Table 4-3 of ECSS-E-ST-10-12C standard [24]. N-channel MOSFETs can be affected by SEB or SEGR and p-channel MOSFETs can only affected by SEGR out of the aforementioned destructive single event effects as described in ECSS-E-HB-10-12A [25]. In SEB an n-channel MOSFET, which is in cut-off mode, is struck by a heavy-ion and, due to the deposited charge, turned on if the charge is sufficient [25]. In SEGR charge delivered by a heavy-ion strike on the gate terminal is sufficient to cause current to be conducted through the gate oxide [25]. SEGR is always destructive and the chance of it occurring can be decreased by using the component within safe operating point area by de-rating the maximum component parameters [25].

United States Department of Defence catalogued the possible failure modes of MOSFETs and their probabilities in respect to one another [22]. The failure modes from the electronic reliability handbook by the Department of Defence are listed in Table 4.2.

Table 4.2 MOSFET failure modes and probabilities [22]

Failure	**Probability**
Short-circuit	0.51
Output Low	0.22
Parameter Change	0.17
Open Circuit	0.05
Output High	0.05

RUAG Space Finland has reviewed passivation functions with MOSFET implementation and proposed several methods in which the transistors could be used in passivating the spacecraft [20]. It is possible to use MOSFETs in battery, solar array and main bus levels. MOSFETs can disconnect the battery and disconnect or short-circuit the solar array or main bus. Due to the short-circuit being the highest failure probability of MOSFET, it was initially recommended that the passivation function utilizing MOSFETs to be designed to have the transistors in saturation mode during the passivation which would put the transistor as the short-circuiting component of the system [21]. Linear mode

failure remains a risk if the transistor is used in short-circuiting passivation function however due to the voltage of the passivated system falling low enough to go below the threshold voltage of the MOSFET. If a MOSFET is designed to disconnect a power line by being in cut-off mode, the transistor would be in series with the power line. The on-resistance of the transistor would cause power dissipation in the series configuration.

In the long-term component behaviour analysis conducted by RUAG Space Finland the pros and cons of MOSFET usage in the passivation were documented [21]. The advantages of using MOSFETs in passivation function are the small size and weight of the transistors which makes it possible to implement the passivation using the internal functions of the PCDU and the use of existing PCDU components. MOSFETs are also already space qualified and make the cancellation of the passivation possible. The disadvantages of using MOSFETs is that the transistors are temperature and radiation sensitive, long term behaviour of MOSFETs is not properly known, the use of MOSFETs could possibly increase the power dissipation during mission. The fact that MOSFETs are licensed components may also increase the price of the system.

4.3 Diodes

Diodes are semi-conductor devices that conduct current in only one direction. They have only anode and cathode terminals. When forward voltage over diode is sufficiently high to overcome the electric field in the depletion region of the pn-junction the diode conducts forward current. If the diode is reverse biased, only negligible reverse current is leaked through. Due to diodes not having control terminals it is not possible to passivate the system using the diodes alone.

Diodes are sensitive to radiation and mainly affected by total ionising dose and displacement damage [24][26]. According to test results presented in NEPP Electronic Technology Workshop by Megan C. Casey et al. reverse biased silicone schottky diodes are additionally vulnerable to single event effects [27]. Diodes have three failure modes according to electronic reliability handbook created by United States Department of Defence. The failure states and their probabilities according to the handbook are listed in Table 4.3 [22].

Table 4.3 Diode failure modes and their probabilities [22]

Failure	Probability
Short-circuit	0.51
Output Low	0.29
Parameter Change	0.2

Due to diodes not having any form of input terminal for control, they must be used in conjunction with other devices in passivation function. Possible use of diodes is segregation of power levels in passivation function. One such use is having diodes separate the solar array power from PCDU and battery.

4.4 Bypass Switches

Bypass switch is an electrically initiated one time switch. Inside the switch is a spring loaded plunger with several precious metal plated electrical contacts in single-pole-double-throw configuration. The plunger is held in place by a split-spool. Once the switch is activated the split-spool is split and the plunger moves inside the housing and changes which terminals are connected to one another.

Bypass switch can typically have four switch configurations, which are normally open contacts, normally closed contacts, make-before-break and break-before-make. Simplified operation of a make-before-make and break-before-make types of bypass switches is illustrated in Figure 4.2.

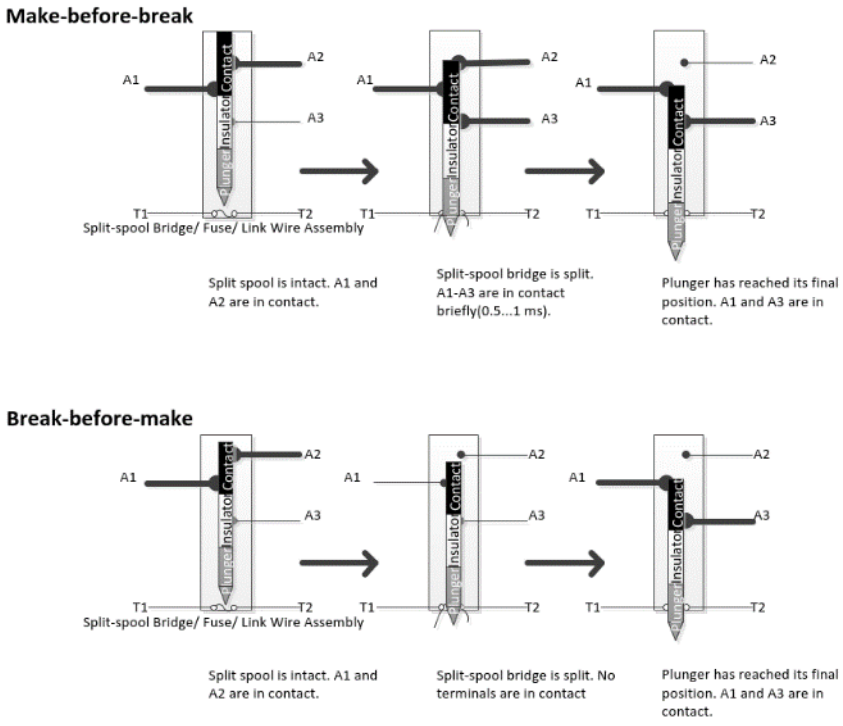


Figure 4.2 Bypass switch make-before-break and break-before-make basic operation principle

The subassembly of the split-spool includes two halves which are wound together tightly with a restraining wire which is terminated in a bridge wire connecting two terminals at the electrical interface of the device. Such terminals are denoted as T1 and T2 in Figure 4.2. Due to the winding, the wire prevents the axial motion of the plunger. Once sufficient current passes through the bridge wire from the terminals, the wire breaks under the

applied tension load. Breaking of the bridge wire allows the restraining wire to unwind and the spool halves to separate which releases the spring-pre loaded plunger. Operation of the split-spool illustrated in Figure 4.3.

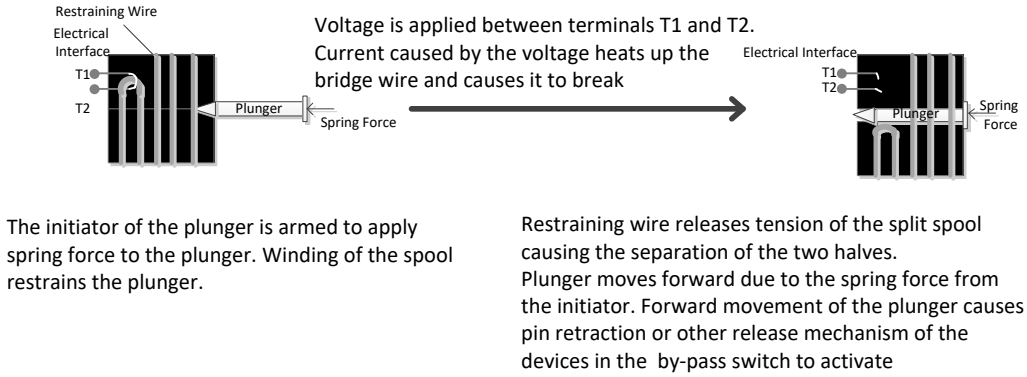


Figure 4.3 Split-spool operation

Unlike in the cases of relays, diodes and MOSFETs, there are no clear statements of bypass switch failure modes in the electronic reliability design handbook [22]. Some possible failure modes have been listed in the component long term behaviour analysis done by RUAG Space Finland which are defined in Table 4.4 [21].

Table 4.4 Possible failure modes of bypass switches [21]

Functional part	Cause	Failure	Effect
Spring	Ageing	Split spool not separated due to fatigued spring	No switching, wrong state of contacts after actuation
Split-spool/plunger	Temperature Mechanical Ageing	Plunger stuck to split spool	No switching, wrong state of contacts after actuation
Restraining wire	Mechanical	Break of restraining wire	Unwanted switching
Sliding contact	Ageing Temperature	Sliding contact resistance increased	Second effect failure due to increased power dissipation
	Temperature Mechanical Ageing	Lubrication quality worsens Sliding contact stuck	No switching, wrong state of contacts after actuation
Screw contacts	Temperature Mechanical Ageing	Screw contact open	Open circuit
	Temperature Mechanical Ageing	Screw contact resistance increased	Second effect failure due to increased power dissipation
Bridge wire	Ageing High Temperature	Split spool not separated due to the increase of wire resistance	No switching
	Low temperature	Split spool not separated due to the heat of bridge wire not being high enough	No Switching
	Mechanical	Break of bridge wire	Unwanted switching

According to the passivation function implementation review done by RUAG Space Finland bypass switches are usable on several levels of the passivation function [20]. Bypass switches can be used in battery, solar array and main bus levels of the passivation function. The bypass switch is used to discharge or short-circuit the power line to which the switch is connected to. It is also possible to disconnect the battery using the bypass switch.

With respect to shock the actuation of bypass switch is considered gentle. Lubrication is required to the sliding contact to fulfil actuation after long time in space. Testability of the battery bypass switches is limited due to the device needing to be field or factory refurbished by replacing the split spool initiators. The test of final flight model of the split-spool initiator is impossible. The design and construction of bypass switch assure

that the probability of bounce is very unlikely during high dynamic loads during satellite launch.

The pros and cons of the possible use of the bypass switch in the passivation function were documented by RUAG Space Finland [21]. The advantages that the use the bypass switches provides are the switches being completely mechanical constructions, the switches being very reliable, the switches not being radiation sensitive, the switches having very low on-resistance and very high current switching capability. Bypass switches are also very easy to control and have a pyro equivalent firing circuit. The disadvantages of using bypass switches are poor testability due to the need to replace the split-spool initiators after every switching action, the inability to test the flight models of the split-spool initiators requiring a Lot Acceptance Test (LAT). The mass of the bypass switches is also large compared to other components. Due to the fact that bypass switches are designed to short battery cells, the switching voltage rating of the switches may not be enough for the passivation function requiring high voltage tolerance for example if the passivated component was a solar array or a battery.

4.5 Cable Cutters

Cable cutter operates by utilizing pyrotechnic actuation. Current causes the pyrotechnic device to actuate and after the reaction the cable to be cut with a sharp knife. Typically cable cutter consists of body, piston, anvil, a cutter blade or knife and an initiator actuator. To cut the cable, first an electrical current pulse is provided to the initiator actuator igniting the explosive charge in the actuator. The pyrotechnical reaction pushes the piston which is connected to the cutter-knife toward the anvil. The cable between the anvil and the knife gets cut and is pulled apart by the tension force. The typical operation of the cable cutter is illustrated in Figure 4.4.

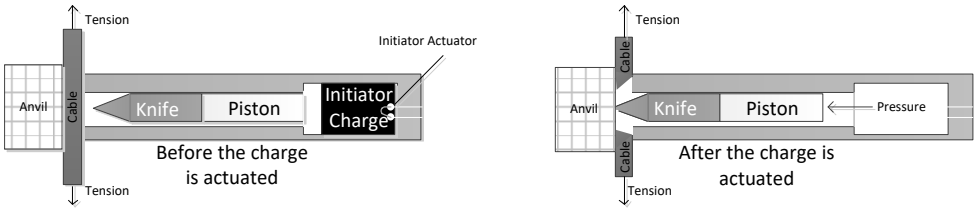


Figure 4.4 Cable cutter operation

Initiator typically has two pins between which the bridge wire is located. Once sufficiently high current is passed through the bridge wire for sufficient time, it heats up, melts and ignites the charge.

If the cut wire is shielded and contains both supply and return powers, it is possible that the powers are short-circuited after the cable is cut. The short-circuit example is illustrated in Figure 4.5.

Figure 4.5 Wires are short-circuited after the cable is cut

In failure modes and effects analysis done by ECSS the failure states of the pyrotechnic devices were listed [28]. The failure states that apply to the initiators in cable cutters from the analysis are in Table 4.5.

Table 4.5 Failure modes of pyrotechnic devices [28]

Device Type	Failure Mode
Initiators	Open-Circuit
	Short-Circuit between Terminals
	Short-Circuit from Terminals to the Structure

In the component long term behaviour analysis done by RUAG Space Finland it was concluded that there are no clear statements for the probabilities of failure modes of the initiator actuators or the cable cutters [21]. In that analysis a possible failure and End-of-Life (EoL) parameter drift list was made. The list is presented in Table 4.6.

Table 4.6 Possible failure modes of cable cutters [21]

Functional part	Cause	Failure	Effect
Charge	Ageing Temperature	Charge powder is not ignited	Cable is not cut
	Ageing Temperature	Pressure force is too low due to charge powder not being ignited properly	Cable is only partially cut
Piston	Temperature Mechanical Ageing	Piston is stuck	Cable not cut or cable only partially cut
Initiator Bridge Wire	Mechanical Temperature cycling	Bridge wire is broken so charge is not ignited	Cable is not cut
	Mechanical Temperature cycling	Weld spot is broken so charge is not ignited	Cable is not cut
	Temperature Ageing	Bridge wire resistance has changed so charge is not ignited	Cable is not cut
Cable	Temperature Mechanical Ageing	Loss of cable tension	Cable halves are not separated properly

Cable cutters can be used in solar array level of the passivation function. The cable cutters can disconnect the solar array from the spacecraft main bus once the passivation has been initiated.

The advantages and disadvantages of the use of the cable cutters in passivation function were listed by RUAG Space Finland [21]. The advantages of using cable cutters in passivation function are the cable being physically separated and the ease to add the cable cutter to power systems since the cutter does not require extra box or a power circuit. The disadvantages are that the cable cutter is not testable, the initiator of the cutter is life-time limited, the explosives used in the operation of the cutter pose safety problems, the powder in the initiator may include carcinogenic compound which would possibly violate Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH) – regulations, the wires being possibly short-circuited after the cutting of the cable, the cancellation of the passivation not being possible and the mass of the cable cutter being

large. The cable-cutter is also not space qualified and increases the cost of the system due to licensing. Integration ease or difficulty depends on the satellite, being particularly difficult on large spacecraft.

4.6 Summary

The switches with which to passivate the spacecraft can be implemented by using relays, MOSFETs, bypass switches and cable cutters. Diodes can be utilized in helping the passivation function along with a switch component. The compiled list of advantages and disadvantages of each of the components is in Table 4.7.

Table 4.7 Advantages and disadvantages of the component types

Device	**Advantages**	**Disadvantages**
Relay	Reliability, insensitivity to radiation, ease of testing and control, low on-resistance, possibility to cancel the passivation function, pyro equivalent firing circuit, space qualification	Unknown long term behaviour, contact power ratings being limited, large mass, possibility of magnetic momentum due to the coils
MOSFET	small mass and size, space qualification, possibility to cancel the passivation function, possibility to use existing PCDU components	Unknown long term behaviour Radiation and temperature sensitivity Possibility to increase power dissipation during the mission due on resistance or linear mode licensing costs
Diode	small mass and size	Unknown long term behaviour, temperature and radiation sensitivity, inability to be used independently.
Bypass Switch	very high reliability, completely mechanical construction, insensitivity to radiation, ease of control, pyro equivalent firing circuit, very low on-resistance and very high current switching capability space qualification	Testability is limited, need of LAT for flight split spool initiators, large mass, possibly low switching voltage rating
Cable Cutter	real physical separation of the power lines, ease of inclusivity in power systems	inability to be tested, initiator being life-time limited and the charge of the initiator including harmful materials and being a safety hazard possibility to short-circuit the wires, no space qualification and the inability to cancel the passivation, large mass, licensing cost

The long term behaviour of relays, MOSFETs and diodes is not currently known. The goal of the test implementation of which is proposed this thesis is to determine the long term reliability of those devices based on the defined temperature conditions. One of disadvantages listed for the bypass switches was the unknown switching voltage. The voltage switching test was planned. Cable cutters were not selected for the test due to their inability to be tested.

5 TESTING OF PASSIVATION COMPONENTS

Due to the long lifetime information not being available from the manufacturers of relays and the semiconductor devices, the behaviour of the components in the nominal mission and disposal phase conditions of the spacecraft was planned to be tested in regards to temperature. Due to bypass switch contact voltages only being rated for individual battery cells, the switch is planned to be tested in electrical conditions representing spacecraft solar array and space craft main bus. The detailed test setup for the semiconductors is proposed. In case of relays and bypass switches only the plan for measured electrical parameters is proposed but the test setups are not detailed.

In this chapter the targets of the tests are defined, the tested components are listed and the testing arrangements are detailed. At the start of the test proposal it was foreseen that the semiconductors and relays would undergo thermal cycling test derived from the conditions of the spacecraft in the field. It was also foreseen that switching voltage test would be performed on the bypass switch. An additional high temperature operating life test was planned for the semiconductor devices. Relays were planned to undergo an extended temperature range test after the tests with MOSFETs by using the full temperature range of the thermal chamber within safety considerations. A test setup for the semiconductors which would be able to tolerate the electrical and thermal conditions of the test is detailed after the test definitions.

5.1 Targets of the Temperature based Tests

The target of the full-scale system tests would have been to provide estimations on the conditions of the semiconductors and relays over artificially accelerated temperature conditions over the lifetime of the spacecraft. The switching test of the bypass switch would have evaluated the performance of the switch when the switch was used outside of its rated voltage. Extended temperature test that would have been performed on relays after the original thermal cycling would have helped to estimate the relay performance in extreme temperatures outside the nominal relay temperature ratings.

In the thermal cycling test the components would have been placed in the thermal chamber and the temperature in the chamber would have been cycled from maximum to minimum defined values for a determined duration. In the high temperature operating life test the temperature of the chamber and the semiconductor junction would have been kept at 150 ºC for the test duration. In the extended temperature range test, the temperature range of the thermal chamber would have been set to the maximum and minimum values available to be used without the safety risks for the premises and test equipment.

For the semiconductor and relay thermal cycling test conditions the parameters were obtained using the Coffin-Manson equation, which was modified by Norris-Landzberg for SnPb solder joints [29]:

$$AF = \left(\frac{f_o}{f_t}\right)^{1,9} \left(\frac{\Delta T_t}{\Delta T_o}\right)^{1/3} e^{1414\left(\frac{1}{T_o}-\frac{1}{T_t}\right)}, \quad (4)$$

where AF denotes the acceleration factor, f_o denotes the frequency of cycles in the field, f_t denotes the frequency of cycles in test, ΔT_t denotes temperature excursion in the test in °C or K, ΔT_o denotes temperature excursion in the field in °C or K, T_o denotes the maximum temperature in the field in K and T_t denotes the maximum temperature in the test in K.

Test duration is achieved by dividing the total number of temperature cycles during the satellite operation by the acceleration factor obtained from the Norris-Landzberg equation. Even though the equation does not apply to semiconductors or relays, the test durations obtained by using this equation were determined to simulate the worst case temperature condition approximations of the spacecraft in the field for the purpose of this test.

In high temperature operational life test for the semiconductors, the thermal chamber is set to such a temperature that the junction temperature of the transistors and diodes would have been at 150 °C for the defined duration. The duration of the life test was defined using a version of Arrhenius equation, which is used to calculate the thermal acceleration factors for semiconductor device time-to-failure distributions according to JEDEC definition [30]:

$$AT = e^{\left(\frac{-E_{aa}}{k}\right)\left(\frac{1}{T_o}-\frac{1}{T_t}\right)}, \quad (5)$$

where AT denotes the acceleration factor due to changes in temperature, E_{aa} denotes the apparent activation energy in eV, k is Boltzmann's constant which is $8{,}62*10^{-5}$ eV/K, T_o denotes the maximum temperature in operation and T_t denotes the maximum temperature in the test. The duration of the life test is obtained by dividing the durations of satellite nominal mission phase and disposal phase by their respective acceleration factors.

The extended temperature range test for relays was planned to be performed over a two-day duration with maximum thermal chamber temperature range limited by the safety precautions. For switching test, the bypass switch was planned to switch the voltage that was representative of the possible solar array or main bus voltages in the field conditions.

5.2 Components for the Full-scale Tests

Several space grade relay, MOSFET and diode types and one bypass switch type were selected for testing. Three automotive grade MOSFETs and one automotive grade diode was included in the list of the components that would have been tested. The selection of components for the tests was not finalized during the writing of this thesis and liberties were taken in the selection of the components for tests in this chapter. The selected components, their manufacturer, their case, the quantity of each component are listed in Table 5.1.

Table 5.1 The components selected for the design of the test prototype

Component	Type	Case	Quantity	Manufacturer
F402J2AH	Relay	4PDT	10	Leach
EL 215147AF7099		2PDT	6	Leach
GP250720E0026V 860EM		2PDT	6	Leach
TL26F70		2PDT	6	STPI
STRH100N10HY1	MOSFET	TO-254AA	10	STM
STRH40P10HY1		TO-254AA	10	STM
IRHMS57160		TO-254AA	10	INR
IRHMS67260		TO-254AA	10	INR
JANSR2N7470T1		TO-254AA	10	INR
2N7236		TO-254AA	6	INR
SQJ402EP*		SO-8L	10	Vishay
FDB3652_FO85*		TO-263AB	10	ONSemi
SCTW100N65G2AG*		HIP-247	10	ST
STPS20100C2FYT	Diode	TO254AA	10	STM
45CKQ100		TO-258AA	10	INR
16CYQ100C		TO-257AA	10	INR
STPSC20H065CT*		TO-220AB	10	ST
European non Dissipative Bypass	Bypass Switch	SPDT	2	Soriau

* Automotive grade components

In long-term behaviour analysis of the components performed by RUAG Space Finland the parameters of the components relevant to the passivation were defined [21]. According to the aforementioned list for MOSFETs the passivation relevant electrical parameters are MOSFET Gate-to-Source threshold voltage, Drain-to-Source-on-resistance and Zero-Gate-Voltage-Drain-Current. For relays the electrical parameters relevant to passivation on the list are contact voltage drop with maximum load current, Latch/Reset voltages after long period of maximum load current through contacts (U_L and U_R), Latch/Reset times and Latch/Reset coil resistances. In addition to the aforementioned parameters, relay leakage current between the open contacts would have been measured

in order to determine whether there was a fault in the insulation of the relay. For diodes the reverse leakage current and forward voltage measurements would have been performed in the test. Contact resistance of the bypass switch would have been measured.

The explanations of the parameter denotations and the raw measurement data required to obtain the parameters are listed in Table 5.2. The parameters foreseen to be measured of the each of the components are listed in Table 5.3.

Table 5.2 Parameter descriptions

Parameter	**Description**	**Required Measurement Data**
VD	Contact voltage drop with maximum load current	V_{IN}, V_{OUT}
I_{LEAK}	Leakage current between the relay terminals which are open	$U_{LEAK\_RESISTOR}$, $R_{LEAK\_RESISTOR}$,
U_L/U_R	Latch/Reset voltages after long period of maximum load current through contacts	U_L, U_R
t_L/t_R	Latch/Reset times	$t_{OUTPUT\_STABILIZED\_L}$ $t_{LCOIL\_VOLTAGE\_INPUT}$ $t_{RCOIL\_VOLTAGE\_INPUT}$
R_B	Latch/Reset coil resistances	U_{RCOIL}, U_{LCOIL}, I_{RCOIL}, I_{LCOIL}
V_{GSTh}	MOSFET Gate-to-Source threshold voltage	V_{GS}, V_{DS}
R_{DSOn}	Drain-to-Source-on-resistance with MOSFET being in saturation mode	V_{DS}, I_{DS}
I_{DSS}	Zero Gate Voltage Drain Current with MOSFET being in cut-off mode	I_{DS}
V_F	Forward voltage over the diode	V_F
V_R	Reverse voltage over the diode	V_R
I_F	Forward Current through the diode	I_F
I_R	Reverse leakage current through the diode	I_R
R_{CR}	Contact resistance	V_{IN}, V_{OUT}, I

Table 5.3 Parameters to be measured of each of the components

Type	Model	Parameters to be measured				
Relay	F402	VD	U_L/ U_R	t_L/ t_R	U_B	I_{LEAK}
	EL215					
	GP250					
	TL26					
MOSFET	STRH100N10	V_{GSTh}	R_{DSOn}	I_{DSS}		
	STRH40P10					
	IRHMS57160					
	IRHMS67260					
	JANSR2N7470T1					
	2N7236					
	SQJ402EP					
	FDB3652_FO85					
	SCTW100N65G2AG					
Diode	STPS20100C2FYT	V_F	I_F	I_R		
	45CKQ100					
	16CYQ100C					
	STPSC20H065CT					
Bypass switch	European non Dissipative Bypass	V_{CR}				

From Table 5.2 it can be seen that in order to obtain most of the desired parameters calculations using the raw measurement data are required. The performance relevant parameters shall be calculated with the following formulae in this test:

$$VD = V_{IN} - V_{OUT} \quad (6)$$

$$R_B = \frac{U_{RCOIL}}{I_{RCOIL}} \text{ and } \frac{U_{LCOIL}}{I_{LCOIL}}, \quad (7)$$

$$I_{LEAK} = \frac{U_{LEAK\_RESISTOR}}{R_{LEAK\_RESISTOR}}, \quad (8)$$

$$R_{DSOn} = \frac{V_{DS}}{I_{DS}}, \text{ while FET is in saturation mode,} \quad (9)$$

$$R_{CR} = \frac{V_{IN} - V_{OUT}}{I}, \quad (10)$$

$$t_L = t_{OUTPUT\_STABILIZED\_L} - t_{LCOIL\_VOLTAGE\_INPUT} \quad (11)$$

$$t_R = t_{OUTPUT\_STABILIZED\_R} - t_{RCOIL\_VOLTAGE\_INPUT} \quad (12)$$

where VD is contact voltage drop, V_{IN} is voltage at the input terminal, V_{OUT} is voltage at the output terminal, U_{RCOIL} is voltage over the reset coil, I_{RCOIL} is the current through the reset coil, U_{LCOIL} is voltage over the latch or the main coil, I_{LCOIL} is the current through the latch or main coil, I_{LEAK} is the leak current of the relay between the opened contacts, $U_{LEAK_RESISTOR}$i is the voltage over the leakage current measurement resistor, $R_{LEAK\_RESISTOR}$ is the resistance of the leakage current measurement resistor, R_{DSOn} is

Drain-to-Source-On resistance with MOSFET being in saturation mode, V_{DS} is Drain-to-Source voltage and I_{DS} is Drain-to-Source current, R_{CR} is contact resistance, I is current through the component, t_L is the latching time, $t_{OUTPUT\_STABILIZED}$ is the time when the voltage at the output to which the contact switches to is stabilized, $t_{LCOIL\_VOLTAGE\_INPUT}$ is the time at which the latching coil is energized, t_L is the reset time and $t_{RCOIL\_VOLTAGE\_INPUT}$ is the time at which the reset-coil is energized.

In order to set-up the parameters of the test, component current, voltage and temperature tolerance ratings should be defined. Nominal parameters of the relays that would have been tested are in Table 5.4. Nominal parameters of the MOSFETs that would have been tested are listed in Table 5.5. Nominal parameters for the diodes in the test are in Table 5.**6**. Nominal temperature ranges of all the components that would have been tested in thermal chamber are listed in Table 5.7.

Table 5.4 Nominal relay parameters.

Relay	Contact Voltage (V)	Contact Current (A)	Contacts	Coil Voltage to be used in test (V)	Operate Time (ms max)	Contact Resistance or Contact Voltage Drop at Nominal Contact Current
F402 [31] *	28	15	4	28	15	Initial: 150 mV AL**: 175 mV
EL215 [32]	28	15	2	28	10	Initial: 150 mV AL**: 175 mV
GP250 [33]	50	2	2	26	4	Initial: 50 mΩ AL**: 100 mΩ
TL26 [34]	28	1	2	26	2	Initial: 10 mΩ AL**: 20 mΩ

*F402 is similar to M402 and uses the datasheet of M402

** After life

Table 5.5 Nominal MOSFET parameters

MOSFET	**$V_{DS,max}$ (V)**	**$V_{GS,max}$ (V)**	**$I_{DS,max\ continuous}$ (A)**		**$I_{DSS,max}$ (A)**	**$R_{DSOn,max}$ (Ω)**
			25°C*	**100°C***		
STRH100N10 [35]	100	± 20	48	30	100 µ	0.063
STRH40P10 [36]	-100	± 20	-34	-21	-10 µ	0.075
IRHMS57160 [37]	100	± 20	45	45	25 µ	0.015
IRHMS67260 [38]	200	± 20	45	35	25 µ	0.029
JANSR2N7470T1 [39]	60	± 20	45	45	25 µ	0.0066
2N7236 [40]	-100	± 20	-18	-11	-250 µ	0.22
SQJ402EP [41]	100	± 20	32	32	150 µ	0.0210
FDB3652_FO85 [42]	100	± 20	61	30	250 µ	0.043
SCTW100N65G2AG [43]	650	- 10 to + 22	100	85	100 µ	0.023

*Case temperature

Table 5.6 Nominal diode parameters

Diode	**V_{F10A*}(V)**	**$I_{F,max\ continuous}$(A)**	**$V_{R,max}$(V)**	**$I_{R,\ maximum}$(A)**	
				25°C**	**125°C****
STPS20100C2FYT [44]	0.78	2 x 20 (20 per leg)	100	30 µ	20 m
45CKQ100 [45]	0.74	45	100	800 µ (per leg)	45 m (per leg)
16CYQ100C [46]	0.75	16	100	0.01 m	10 m
STPSC20H065CT 98[47]	2.1	2 x 10 (10 per diode)	650	100 µ	425 µ***

*Forward current of the diodes was selected to be 10 A in the test and forward voltage when the component was closest to conducting 10A was selected from the datasheet.
**Case temperature in for STPS20100C2FYT, junction temperature for other diodes
*** Junction temperature was defined to be 150 °C in the datasheet

Table 5.7 Nominal temperature ranges for the tested components

Type	Component	Minimum T (°C)	Maximum T (°C)
Relay	F402 [31]	-70	125
	EL215 [32]	-70	125
	GP250 [33]	-65	125
	TL26 [34]	-65	125
MOSFET	STRH100N10 [35]	-55	150
	STRH40P10 [36]	-55	150
	IRHMS57160 [37]	-55	150
	IRHMS67260 [38]	-55	150
	JANSR2N7470T1 [39]	-55	150
	2N7236 [40]	-55	150
	SQJ402EP [41]	-55	175
	FDB3652_FO85 [42]	-55	175
	SCTW100N65G2AG [43]	-55	200
Diode	STPS20100C2FYT [44]	-65	175
	45CKQ100 [45]	-55	150
	16CYQ100C [46]	-65	150
	STPSC20H065CT 98[47]	-40	175

In order to achieve a safety margin in the component use in space the nominal parameters of the components need to be de-rated. De-rating is performed in accordance with ECSS-Q-ST-30-11C standard for the nominal mission phase. Due to the nature of the life test, the junction temperature de-rating rules are ignored for that test. Due to STPSC20H065CT having insufficient minimum temperature tolerance the test could be changed in three following ways. The minimum temperature range of the aforementioned diode type could be ignored (risk of damaging the diode is increased), the thermal cycling minimum and maximum temperatures could be reduced (test would be prolonged in this case) changed or STPSC20H065CT could be removed from the tests. Rules applicable to the test according to ECSS-Q-ST-30-11C are listed in Table 5.8. De-rated relay parameters for the test are listed in Table 5.9. De-rated MOSFET parameters for the test are listed in Table 5.10. De-rated diode parameters are in Table 5.11.

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Table 5.8 Derating rules for the selected component types for the tests [48]

Relay	$0.75*I_{CONTACT}$ (less than 50% of qualified switching operations)			$3* t_{OPERATE}$
MOSFET	$0.75* V_{GS}$	$0.8* V_{DS}$	$0.75*I_{DS}$	$T_{j\ max,\ derated}$ is the smaller of (110 °C) or ($T_{j\ max,\ nominal}$ – 40 °C) comparison
Diode	$0.75* V_R$	$0.6* I_D$	$T_{j\ max,\ derated}$ is the smaller of (110 °C) or ($T_{j\ max,\ nominal}$ – 40 °C) comparison	

Table 5.9 De-rated relay parameters

Model	**De-rated Maximum Operate Time (ms)**	**De-rated Maximum Contact Current (A)**
M402	45	11.25
EL215	30	11.25
GP250	12	1.5
TL26	6	0.75

Table 5.10 De-rated MOSFET parameters

MOSFET	**De-rated $V_{DS,\ max}$ (V)**	**De-rated $V_{GS,\ max}$ (V)**	**De-rated $I_{DS,\ max\ continuous}$ (A)**		**De-rated Tj,max(°C)**
			@25°C	**@100°C**	
STRH100N10	80	± 15	36	22.5	110
STRH40P10	-80	± 15	-25.5	-15.75	110
IRHMS57160	80	± 15	33.75	33.75	110
IRHMS67260	160	± 15	33.75	26.25	110
JANSR2N7470T1	48	± 15	33.75	33.75	110
2N7236	-80	± 15	-13.5	-8.25	110
SQJ402EP	80	± 15	24	24	110
FDB3652_FO85	80	± 15	45.75	32.25	110
SCTW100N65G2AG[43]	520	-7.5 to +16.5	75	63.75	110

Table 5.11 De-rated diode parameters

Diode	$I_{F,max\ continuous}$(A)	$V_{R,\ max}$(V)	De-rated Tj,max(°C)
STPS20100C2FYT	2 x 12	75	110
45CKQ100	27	75	110
16CYQ100C	12	75	110
STPSC20H065CT	2 x 6	487.5	110

The current conducted by the relays in the test was planned to be their de-rated maximum current multiplied by the number of contacts of the relays. The total theoretical maximum conducted de-rated current for each of the tested relay types is listed in Table 5.12.

Table 5.12 Theoretical maximum de-rated current of the tested relay types

Model	De-rated $I_{CONTACT}$(A)	Number of contacts	Number of contacts * $I_{CONTACT}$(A)
F402	11.25	4	45
EL215	11.25	2	22.5
GP250	1.5	2	3
TL26	0.75	2	1.5

Due to the total conducted current per relay exceeding the rating of a single contact it was discussed and assumed that the de-rated maximum current value per contact would account for the contact resistance differences of the same individual relay. Thus, it was assumed that the current should not damage the contacts.

5.3 Full-scale test parameters

The tests for each of the components could be divided into four parts. After the PCB (Printed Circuit Board) assembly every parameter listed in Table 5.3 was to be measured. In the first part of the test in the thermal chamber, the parameters relevant to nominal mission phase would have been measured. After the nominal mission phase would have been concluded, the parameters of the thermal cycling and the states of the components changes and the parameters relevant to the disposal phase would have been recorded. After the disposal phase test would have been concluded every listed parameter of the components would be measured once again and compared to the first measurements performed after the assembly. The flow chart of the test is illustrated in Figure 5.1.

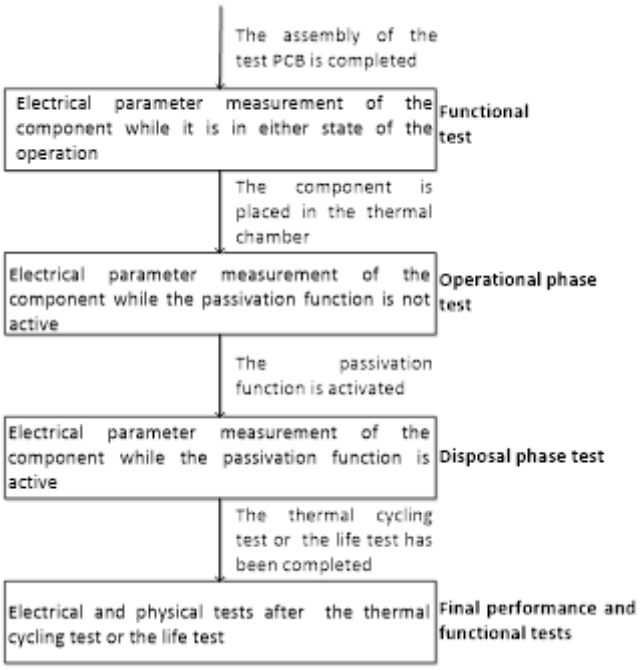


Figure 5.1 Flow chart of the test procedure

The components would have been tested in the following passivation functions: short-circuit of the solar array (SC of SA), disconnection of the solar array (Disconnection of SA), discharge of battery, disconnection of battery and short-circuit of a solar array section (SC of a SA section). The component numbers for each of the tested passivation functions are defined in Table 5.13. The bias conditions of the relays are defined in Table 5.15. The bias conditions of the semiconductors are defined in Table 5.16. The bias conditions of the bypass switches are defined in Table 5.17.

Table 5.13 Passivation functions to be for MOSFETs

Type	Model	Passivation Functions to be Tested
MOSFET	STRH100N10	5 pcs: life test 5 pcs: thermal cycling Disconnection of SA or Battery
	STRH40P10	5 pcs: life test 5 pcs: thermal cycling Disconnection of SA or Battery
	IRHMS57160	5 pcs: life test 5 pcs: thermal cycling Disconnection of SA or Battery
	IRHMS67260	5 pcs: life test 5 pcs: thermal cycling Disconnection of SA or Battery
	JANSR2N7470T1	5 pcs: life test 5 pcs: thermal cycling Disconnection of Battery
	2N7236	3 pcs: life test 3 pcs: thermal cycling Disconnection of SA or Battery
	SQJ402EP	5 pcs: life test 5 pcs: thermal cycling Disconnection of SA or Battery
	FDB3652_FO85	5 pcs: life test 5 pcs: thermal cycling Disconnection of SA or Battery
	SCTW100N65G2AG[43]	5 pcs: life test 5 pcs: thermal cycling Disconnection of SA or Battery

Table 5.14 Passivation functions to be tested for the relays bypass switches and diodes

Type	**Model**	**Passivation Functions to be Tested**
Relay	F402J2AH	5 pcs: SC of SA 5 pcs: Disconnection of SA
	EL215	5 pcs: SC of SA 5 pcs: Disconnection of SA
	GP250	10 pcs: Discharge of Battery
	TL26	10 pcs: Discharge of Battery
Diode	STPS20100C2FYT	5 pcs: life test 5 pcs: thermal cycling SC of a SA section
	45CKQ100	5 pcs: life test 5 pcs: thermal cycling SC of a SA section
	16CYQ100C	5 pcs: life test 5 pcs: thermal cycling SC of a SA section
	STPSC20H065CT	5 pcs: life test 5 pcs: thermal cycling SC of a SA section
Bypass Switch	European non dissipative bypass	2 pcs: SC of SA

Table 5.15 Relay bias conditions

Model	**Nominal Mission Phase**		**Switching Phase**		**Disposal Phase**	
M402	V_{OFF} =50V V_{ON} =5V	I_{OFF} =0A I_{ON} =45A	V_{SWITCH} =28V V_{COIL} =28V	I_{SWITCH} =10A	V_{ON} =5V V_{OFF} =50V	$I_{\_ON}$ =45A $I_{\_OFF}$ =0A
EL215	V_{OFF} =50V V_{ON} =5V	I_{OFF} =0A I_{ON} =20A	V_{SWITCH} =28V V_{COIL} =28V	I_{SWITCH} =10A	V_{ON} =5V V_{OFF} =50V	$I_{\_ON}$ =20A $I_{\_OFF}$ =0A
GP250	V_{OFF} =50V	I_{OFF} =0A	V_{SWITCH} =50V V_{COIL} =26V	I_{SWITCH} =1,5A	V_{ON} =5V	I_{ON} =3A
TL26	V_{OFF} =50V	I_{OFF} =0A	V_{SWITCH} =50V V_{COIL} =26V	I_{SWITCH} =1,5A	V_{ON} =5V	I_{ON} =3A

Table 5.16 Semiconductor bias conditions

Type	**Model**	**Nominal Mission Phase***		**Disposal Phase**	
MOSFET	STRH100N10	V_{ON}=15V V_{DS} =1.32V	I_{DS}=20A	V_{OFF}=80V V_{DS} =80V	I_{DS} =0A
	STRH40P10	V_{ON}=15V V_{DS}= -1.89V	I_{DS}= -15A	V_{OFF}=80V V_{DS} =-80V	I_{DS} =0A
	IRHMS57160	V_{ON}=15V V_{DS}=0.7V	I_{DS}=25A	V_{OFF}=80V V_{DS} =80V	I_{DS} =0A
	IRHMS67260	V_{ON}=15V V_{DS}=0.9788V	I_{DS}=20A	V_{OFF}=80V V_{DS} =80V	I_{DS} =0A
	JANSR2N7470T1	V_{ON}=15V V_{DS}=0.304V	I_{DS}=25A	V_{OFF}=80V V_{DS} =80V	I_{DS} =0A
	2N7236	V_{ON}=15V V_{DS}=-1V	I_{DS}=-6A	V_{OFF}=80V V_{DS} =-80V	I_{DS} =0A
	SQJ402EP	V_{ON}=15V V_{DS}=-2.16V	I_{DS}=20A	V_{OFF}=80V V_{DS} =80V	I_{DS} =0A
	FDB3652_FO85	V_{ON}=15V V_{DS}=0.828V	I_{DS}=20A	V_{OFF}=80V V_{DS} =80V	I_{DS} =0A
	SCTW100N65G2AG	V_{ON}=15V V_{DS}=0.575V	I_{DS}=25A	V_{OFF}=80V V_{DS} =80V	I_{DS} =0A
Diode	STPS20100C2FYT	V_R=75V	I_F=0A	V_{ON}=80V V_F =0.8V	I_F =10A
	45CKQ100	V_R=75V	I_F=0A	V_{ON}=80V V_F=0.74V	I_F =10A
	16CYQ100C	V_R=75V	I_F=0A	V_{ON}=80V V_F=0.74V	I_F =10A
	STPSC20H065CT	V_R=75V	I_F=0A	V_{ON}=80V V_F=2.1V	I_F =10A
V_{GS}(N-MOSFET)		**12V**		**0V**	
V_{GS}(P-MOSFET)		**-12V**		**0V**	

*V_{DS} = I_{DS} * $R_{DSOnmax}$, $R_{DSOnmax}$ is maximum on-resistance found in the respective datasheets of the devices in case of junction temperature being 150 °C.

Table 5.17 Bypass switch bias conditions

Model	**Pre Switching Phase**		**Switching Phase**		**Post Switching Phase**	
Souriau BP-Switch	V_{OPEN}=35V	I_{OPEN} =0A	V_{SWITCH} =30V	I_{SWITCH} =60A	V_{CLOSED} =5V	I_{CLOSED} =60A

Components tested in the SC of SA and SC of Battery passivation functions would be in open state (relay or bypass switch not conducting) with open state voltage, which was defined in the bias conditions, between the non-conducting terminals. Once the simulated nominal mission phase would have been concluded, the tested component would be switched to closed state and begin conducting initially with switching voltage and current. Once the relay is switched the relay would stay closed in the disposal phase conducting the current defined in the bias conditions. Voltage would be lowered for the disposal phase in order to decrease power dissipation.

Solar array or battery disconnection passivation function is simulated was to be simulated as the inverse of the short-circuit functions. The component would have conducted the current defined by the bias conditions during the nominal mission phase. Once the passivation function would have been activated the relays would have been switched with switching voltage to open state and MOSFETs would enter cut-off mode. After the switching the components would remain in open state with open state voltage across the open terminals until the conclusion of the disposal phase. The voltage is defined in the bias conditions.

The diodes used in the SC of a SA section passivation function were planned to be to be reverse-biased with the voltage defined in bias conditions during the nominal mission phase. Once the nominal mission phase would have been concluded and passivation function activated the diodes were defined to conduct 10 A.

Two of the relay types were planned to be simulated in the conditions resembling battery discharging passivation functions due to the low current ratings of the relays in comparison to the other relays in test. In the nominal mission the relays would have been open state with open voltage between the open terminals defined in the bias conditions. After the nominal mission phase would have passed the relay would have connected the discharging resistors to the simulated battery with the voltage and current defined in the bias conditions. After switching the relays would have conducted the discharge current defined in the bias condition for the disposal phase.

The test of the components was foreseen to be started with thermal cycling test. Once the nominal mission phase of the thermal cycling test would have been concluded and

MOSFETs would have been set to open state (cut-off state), some of the equipment was planned to be transferred to the life test. Life test thus would have begun later than the thermal cycling test. The timing of the parameter measurement is illustrated in Table 5.18.

Table 5.18 Timing of parameter measurements

Component type	Tests to be performed	
Relay	Before thermal cycling: VD, I_{LEAK}, U_L/U_R, t_L/t_R and R_B measurements Thermal cycling (parameter measurements in room, minimum and maximum temperatures and every 500 hours): 1. During nominal mission phase: VD and I_{LEAK} measurements 2. During the change of phase from nominal mission to disposal(switching phase): t_L measurement (voltage and current during switching shall be recorded in addition to the switching time) 3. During disposal phase: VD and I_{LEAK} measurements 4. During the end of the disposal phase(extended temperature test): VD and I_{LEAK} measurements After thermal cycling: VD, I_{LEAK}, U_L/ U_R, t_L/ t_R and R_B measurements	
MOSFET	Before the test: V_{GSTh}, R_{DSOn} and I_{DSS} measurements Life test(parameter measurements every 500 hours) 1. During nominal mission phase: R_{DSOn} measurement 2. During disposal phase: I_{DSS} measurement After the life test: V_{GSTh}, R_{DSOn} and I_{DSS} measurements	Before the test: V_{GSTh}, R_{DSOn} and I_{DSS} measurements Thermal cycling (parameter measurements in room, minimum and maximum temperatures and every 500 hours): 1. During nominal mission phase: R_{DSOn} measurement 2. During disposal phase: I_{DSS} measurement After the thermal cycling: V_{GSTh}, R_{DSOn} and I_{DSS} measurements
Diode	Before the tests: V_F and I_D measurements in 80V/10A bias and I_R measurement in 75V reverse bias. Life test (parameter measurements every 500 hours 1. During nominal mission phase: I_R measurement 2. During disposal phase: V_F and I_D measurements After the life test: V_F and I_D measurements in 80V/10A bias and I_R measurement in 75V reverse bias.	Before the tests: V_F and I_D measurements in 80V/10A bias and I_R measurement in 75V reverse bias. Thermal cycling (parameter measurements in room, minimum and maximum temperatures and every 500 hours 1. During nominal mission phase: I_R measurement 2. During disposal phase: V_F and I_D measurements After the thermal cycling: V_F and I_D measurements in 80V/10A bias and I_R measurement in 75V reverse bias.
Bypass switch	Switching test at room temperature 1. Bypass switch is in open-state in 35V 2. Voltage is lowered to 30V and bypass switch shall short circuit the power sources with current limit being 60A. 3. Power source voltage shall be lowered to 5V: R_{CR} measurement	

The tests would have been performed in RUAG Space Finland premises using equipment provided by RUAG Space Finland. Block diagrams of the planned test arrangements (with some data redacted) in different phases and tests are shown in Figure 5.2, Figure 5.3, Figure 5.3, Figure 5.4 and Figure 5.5.

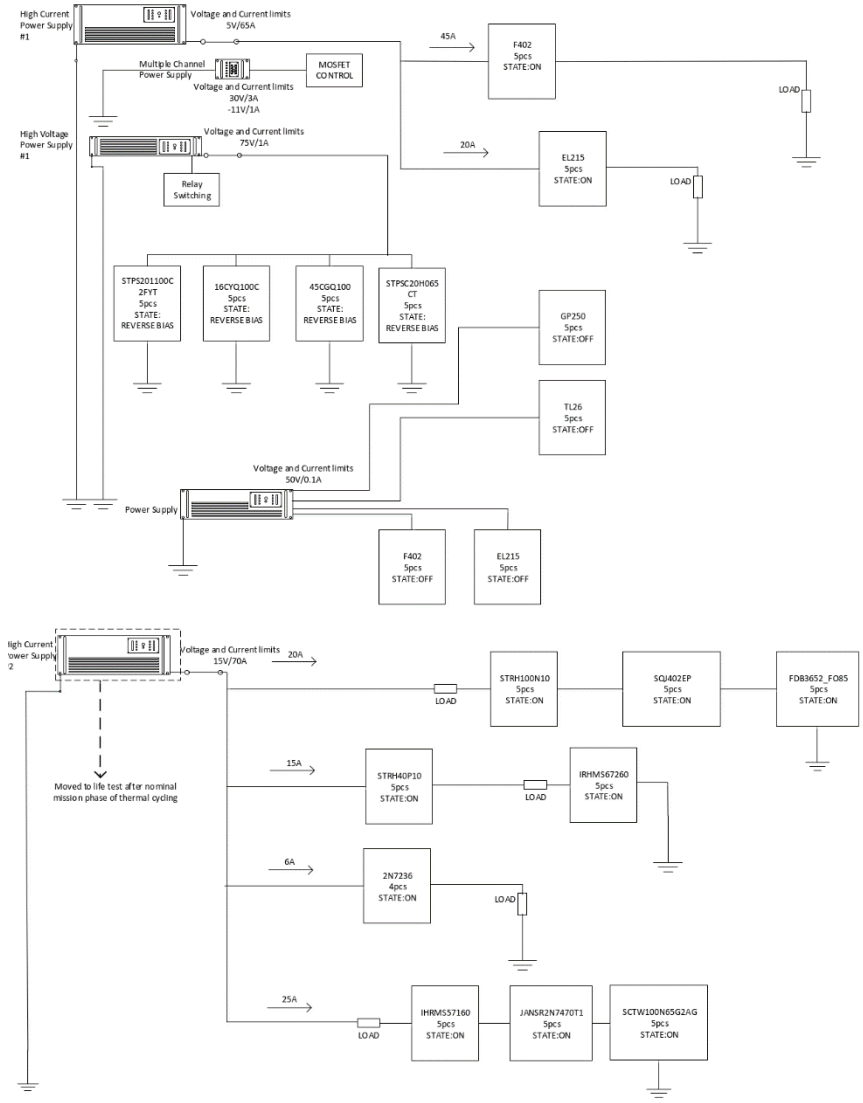


Figure 5.2 Test power usage in nominal mission phase of the thermal cycling test

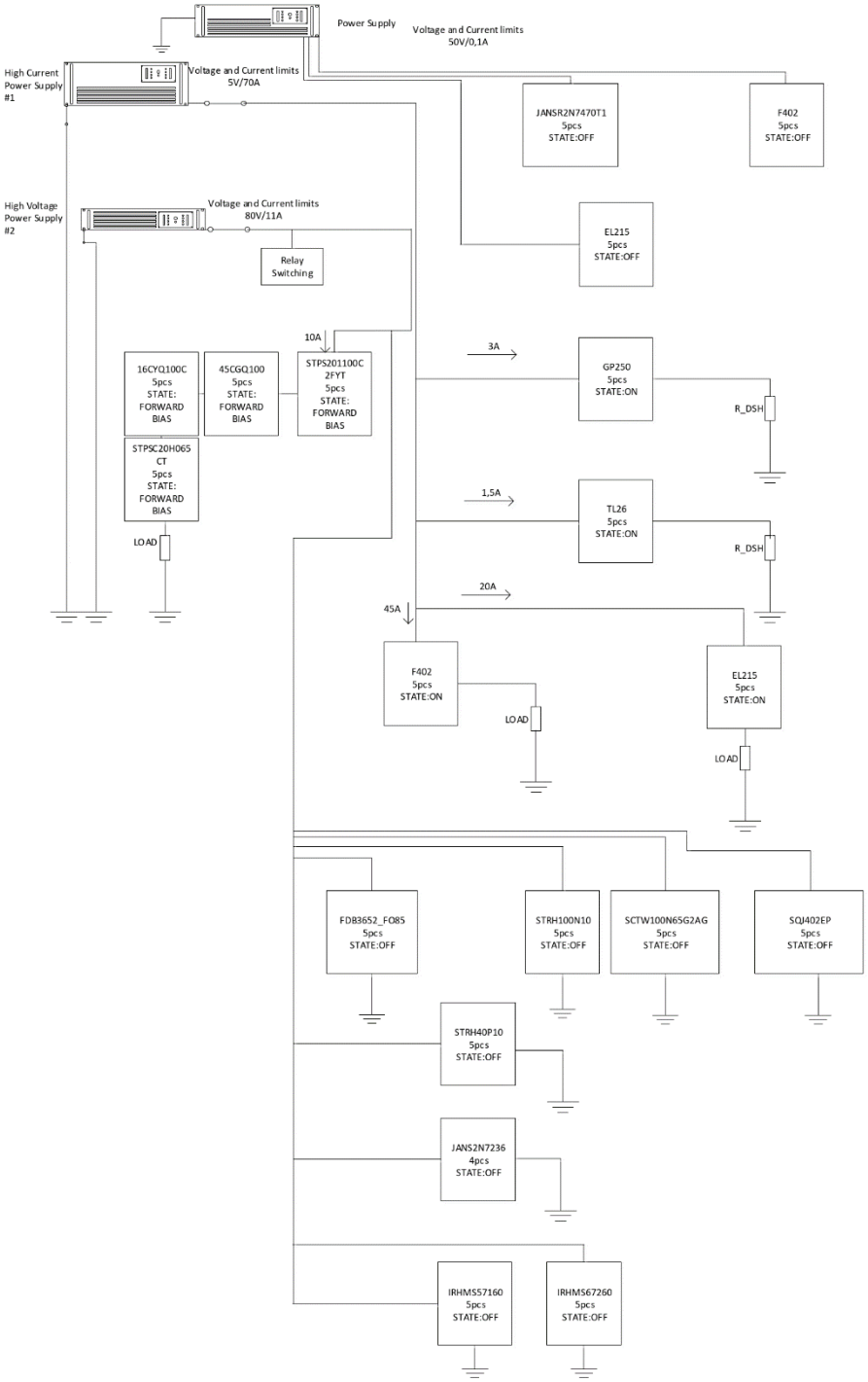


Figure 5.3 Test power usage in disposal phase of the thermal cycling test

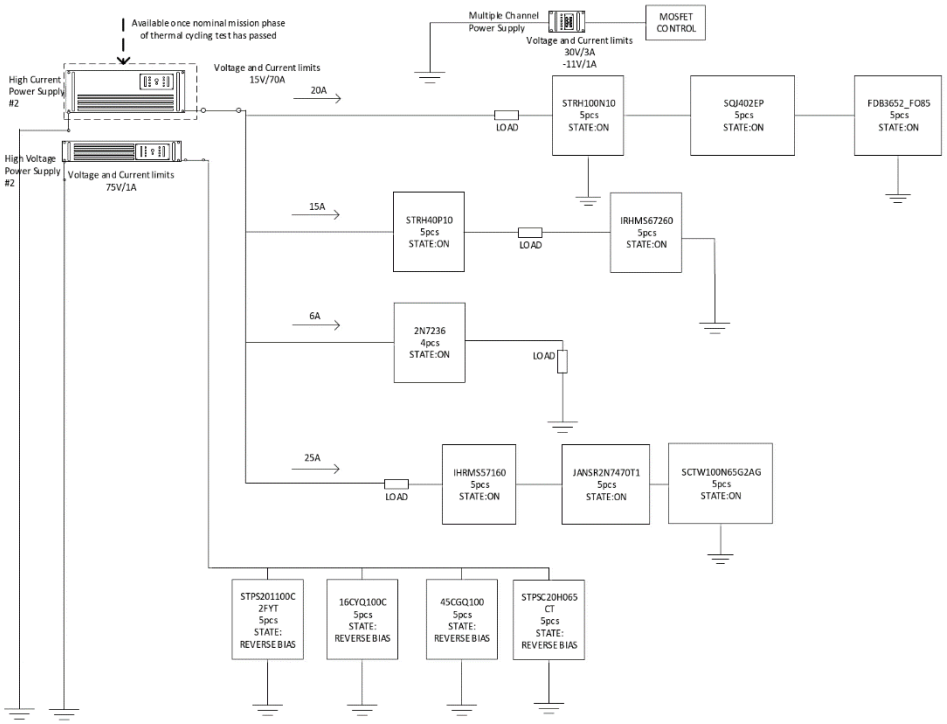


Figure 5.4 Test power usage in nominal mission phase of the life test

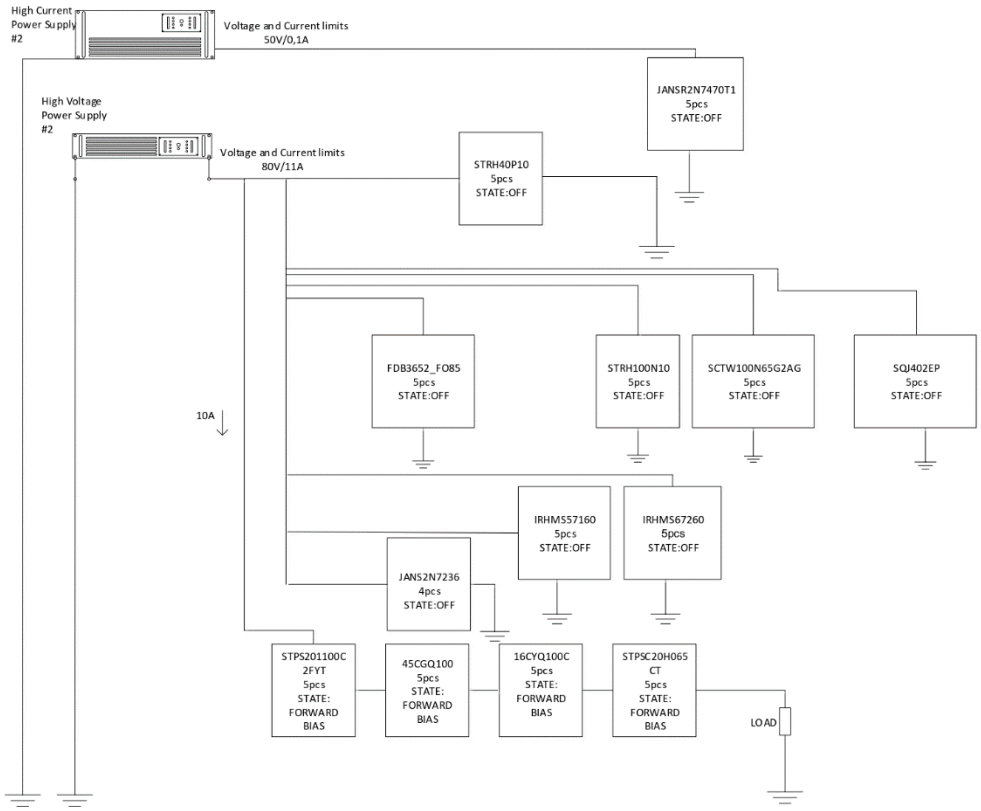


Figure 5.5 Test power usage in disposal phase of the life test

Due to the large current requirement the relays of the same types would have been connected in series to a high current capable power source during the state that relays were planned to be conducting, which is shown by On-state in Figure 5.2 and Figure 5.3. During the state when the relays would not have been conducting, which is shown as Off-state in Figure 5.2 and Figure 5.3, the relays would have been connected in parallel to a high voltage capable power source. The control of relays was planned to be implemented using a relay type specific front resistor for the coil in series with a pushbutton. By pushing the button the coil would have been energized switching the relay contacts. Due to all the relays in the test being latching type, coil would not have to be energized outside of switching phase. In the test, the switching of each individual relay would have been monitored in order to obtain the latch time, voltage and current waveforms. After switching of a single relay, connections would have been rearranged using jumper barrier blocks and screw connectors on the measurement PCB and pushbuttons on an external breakout box.

Due to the large current requirement during the nominal mission phase the MOSFETs would have been connected in series based on the Drain-to-Source current capability as illustrated in Figure 5.2 and Figure 5.4. The current that would have been passed through the series connection was planned to be the smallest de-rated Drain-to-Source of the transistors in the series connection. Once the passivation would have begun in the disposal phase, the transistor would have been connected to a high voltage capable power source in parallel configuration as illustrated in Figure 5.3 and Figure 5.5. The MOSFETs would have been kept in saturation mode using Gate-to-Source control voltage during the nominal mission phase. Due to the series connections of the MOSFETs the gate voltages would have to be adjusted to individual transistors based on the source voltages. Initially the Gate-to-Source voltages were planned to be provided by voltage division based on the Drain-to-Source-on-resistances of the transistors in the series connections. Due to the R_{DSOn} changing based on the junction temperature however, the control voltage implementation plan was changed to be operational amplifier based. When the passivation would have been activated the gate and source terminals of the MOSFETs would have been shorted and Gate-to-Source voltage controlling circuit removed. The connections would be adjusted using screw connectors and jumper barrier blocks on the measurement PCBs and pushbuttons on the external breakout boxes.

During nominal mission phase, the diodes would have been connected to the power source in reverse bias configuration in parallel as illustrated in Figure 5.2 and Figure 5.4. After the activation of the passivation diodes of the test would have been connected in series and would have conducted 10 A while being forward biased as illustrated in Figure 5.3 and Figure 5.5. The connections of the diodes would have been rearranged using pushbuttons on the breakout boxes and jumper barrier blocks and screw connectors on the measurement PCBs.

The lengths of the tests that would have been performed to the selected components were defined inserting pre-defined field conditions of the satellites in the Norris-Landzberg and Arrhenius equations (formulae 4 and 5 respectively). The field conditions of the satellites are defined in Table 5.19. By defining the minimum and maximum temperatures in the thermal cycling test and using cycles per day as frequency and inserting those into Formula 4 the length of the thermal cycling test can be derived. The thermal chamber temperature ranges, daily cycle quantities and test lengths are in Table 5.20.

Table 5.19 Field conditions defined for the temperature based tests

Phase	**Length**	**Thermal Conditions**	**Junction Temperature**	**Number of Cycles**
Nominal mission phase	15 years	15 cycles per day from +20 °C to +40 °C	40 °C	82125
Disposal phase	25 years	15 cycles per day from +60 °C to +80 °C	70 °C	136875
Total Cycles				219000

Table 5.20 The parameters for thermal cycling

Tested Phase	**Minimum T**		**Maximum T**		**ΔT**	**Test Cycles per day**	**Total Test Cycles**	**Duration (Days)**
	(K)	**(ºC)**	**(K)**	**(ºC)**				
Nominal Mission Phase	-55	218.15	110	-55	165	23	752.51	32.71
Disposal Phase	-55	218.15	125	-55	180	23	1543.30	67.1
Total Duration							**Days**	99.8
							Months	3.3

The planned duration of the life test was obtained by inserting the defined junction temperature in the test as the maximum test temperature, selected apparent activation energy, and the defined junction temperatures in the field conditions as the maximum temperature in operation into Formula 5. The aforementioned parameters and the derived life test duration are in Table 5.21.

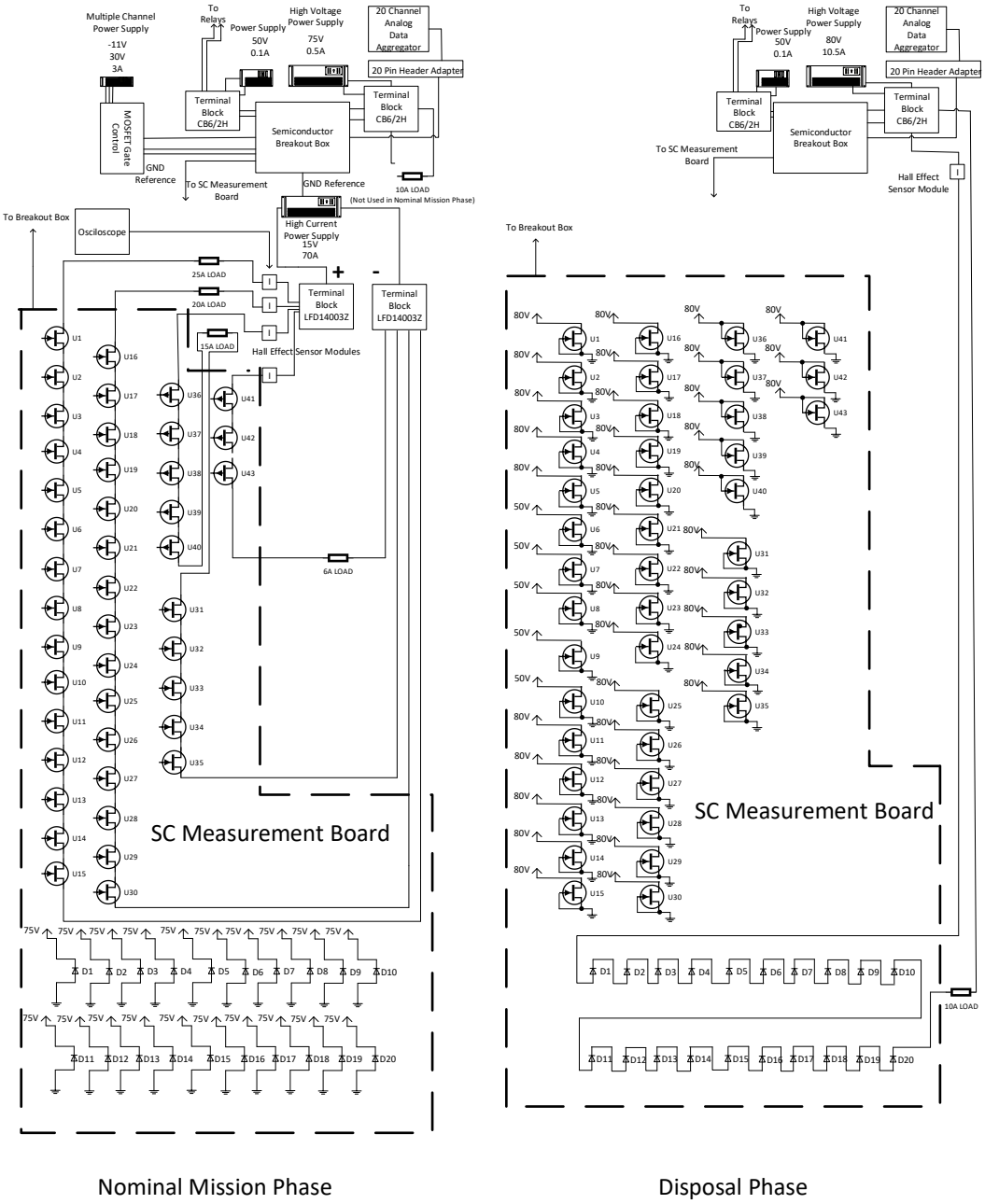
Table 5.21 Life test parameters

Tested Phase	Apparent Activation Energy (eV)	Test T_{JMAX}		Test Duration	
		K	°C	Days	Months
Nominal Mission Phase	0.6	423.15	150	16.86	0.562
Disposal Phase		432.25	150	196.53	6.551
Total Duration (Months)					7.11

In order to optimize the power consumption the high current capable power supply would have been used in both the thermal cycling and life tests. Consequently, the total duration the temperature based testing would have been the sum of the duration of nominal mission phase of the thermal cycling test and both phases of the life test. The total duration would be slightly over eight months. Due to long lead times of the components, the test plan was still in draft phase and not approved at the time of writing this thesis. Due to the life test being defined to be based on the junction temperature and different components having different thermal properties, electrical bias properties and passivation functions, the junction temperatures need to be equalized. The plan for the thermal equalization system was not in the scope of this thesis but may be needed in the test implementation.

5.4 Full-scale test setup of the semiconductors

Schematic and layout of the semiconductor test setup was designed independently from RUAG Space Finland after Master of Science thesis contract had expired. Block diagram of the connections of the designed system during nominal mission phase and disposal phase using available assets of Microsoft Visio is illustrated in Figure 5.6. The reference designators for the semiconductors in Figure 5.6 are defined in Table 5.22. The designed main components of the system are the breakout box, board of devices under test (SC Measurement Board) and MOSFET gate control board. Schematics and layouts were designed using Mentor PADS. Most of the component models were created based on the package dimensions from the datasheets of the devices. In order to separate signals of the same potential for the purposes of measurement and grounding, a component called MEAS_PT was created in pads. MEAS_PT is a short circuit connection with two square pads placed next to one another. The created part caused an error in Design Rule Check (DRC) in PADS. Each reported error of the DRC was carefully examined and if the cause for the error was determined to be MEAS_PT, ignored.



Nominal Mission Phase

Disposal Phase

Figure 5.6 Semiconductor test setup

Table 5.22 Reference designators used for the semiconductors planned to be tested

Ref-Des	Model	Test Current	Series Connection Ref-Des
U1-U5	IRHMS57160	25A	A
U6-U10	JANSR2N7470T1	25A	A
U11-U15	SCTW100N65G2AG	25A	A
U16-U20	STRH100N10HY1	20A	B
U21-U25	SQJ402EP	20A	B
U26-U30	FDB3652_FO85	20A	B
U31-U35	IRHMS67260	15A	C
U36-U40	STRH40P10HY1	15A	C
U41-U43	2N7236	6A	D
D1-D5	STPS20100C2FYT	10A	E
D6-D10	45CKQ100	10A	E
D11-D15	16CYQ100	10A	E
D16-D20	STPSC20H065CT	10A	E

Clearance rules in the layout designs of the test system were partly based on ECSS-Q-ST-70-12C [49]. On page 105 in Table 13-7 of the standard 570 µm is the largest insulation distance requirement for external traces on PCBs with voltage peaks between 50V and 100V. The insulation distance requirement was selected as the clearance rule for traces and copper areas in design. On page 116 in Table 14-1 of the standard the track distance between board edge and track is defined as 0.7 mm. In Table 14-2 of the standard on page 118 the recommended distance between component bodies was defined as 1.0 mm. 1.0 mm was also selected as the drill-to-drill distance in the design. On page 119 of the standard Table 14-3 defines the distance between pads of PTH on component side and pads of leaded SMT devise as 0.5 mm which was selected as every other clearance rule not defined previously in this paragraph. The design rules used for printed circuit boards of this thesis are in Figure 5.7. The minimum, recommended and maximum trace widths are millimetre conversions of 15 and 250 mils.

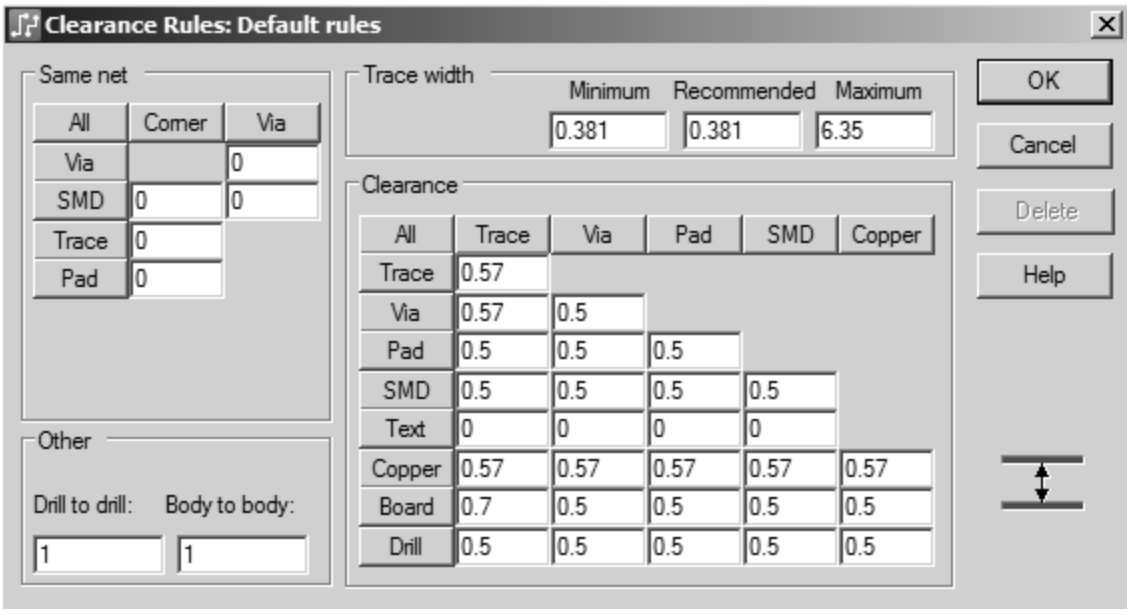


Figure 5.7 Clearance rules for the designed layouts. Dimensions in mm

In ECSS-Q-ST-70-12C clause 13.6.1 [49] the current rating of PCBs is stated to be based on IPC-2152 standard. Due to IPC-2152 being behind a paywall [50], the interpretation present in ECSS-Q-ST-70-12C was used in this thesis. According to ECSS-Q-ST-70-12C the temperature increment of tracks with respect to electric substrate should be equal or less than 5 °C and temperature of tracks should be less or equal to 85 °C. The track temperature requirement is not possible to be met due to test temperatures being over 100 °C in the case of thermal cycling test. Equations used to calculate current rating and cross sectional area (solved from the current rating equation) based on temperature increment in Annex D of ECSS-Q-ST-70-12C [49] are the following:

$$I = k_0 \Delta T^{k_1} (c_1 A)^{\frac{1}{m_0 \Delta T^{m_1}}}, \tag{13}$$

$$A = \frac{1}{c_1} \left(\frac{I}{k_0 \Delta T^{k_1}}\right)^{\frac{1}{m_0 \Delta T^{m_1}}}, \tag{14}$$

where ΔT is temperature increment of tracks in °C, I is current rating in Amperes, A is cross sectional area in mm^2, c_1 is a conversion factor for mm^2 to mils, k_0, k_1, m_0 and m_1 are standard specific constants. Values for the standard specific constants in case of IPC-2152 and c_1 are defined in Table 5.23.

Table 5.23 Constants used in Formulae 13 and 14 [49]

c_1	1550
k_0	0.0756
k_1	0.4375
m_0	0.5000
m_1	0.0301

Copper weight is typically expressed in oz. One oz. is equivalent to 35 µm thick copper layer. Track width requirements calculated with Formula 14 using constants in Table 5.23 and 5 ^{o}C temperature increment are defined in Table 5.24. One millimeter is approximately 39.37 mils. Obtained trace widths converted to mils are in Table 5.25.

Table 5.24 Trace widths with different currents and copper weights with 5 ^{o}C increment

		Trace width(mm)						
		oz	**oz**	**oz**	**oz**	**oz**	**oz**	**oz**
I(A)	**A(mm^2)**	**0.500**	**1.000**	**2.000**	**3.000**	**4.000**	**5.000**	**6.000**
0.100	0.0003	0.016	0.008	0.004	0.003	0.002	0.002	0.001
0.500	0.006	0.353	0.176	0.088	0.059	0.044	0.035	0.029
1.00	0.023	1.321	0.660	0.330	0.220	0.165	0.132	0.110
2.00	0.087	4.948	2.474	1.237	0.825	0.619	0.495	0.412
6.00	0.702	40.137	20.069	10.034	6.690	5.017	4.014	3.345
15.0	4.026	230.034	115.017	57.508	38.339	28.754	23.003	19.169
20.0	6.965	397.972	198.986	99.493	66.329	49.746	39.797	33.164
25.0	10.655	608.845	304.422	152.211	101.474	76.106	60.884	50.737

Table 5.25 Trace widths with different currents in mils

	Trace width(mils)						
I(A)	**oz=0.5**	**oz=1**	**oz=2**	**oz=3**	**oz=4**	**oz=5**	**oz=6**
0.1	0.65	0.323	0.162	0.108	0.081	0.065	0.054
0.5	13.88	6.94	3.47	2.31	1.74	1.39	1.16
1	52.00	26.00	13.00	8.67	6.50	5.20	4.33
2	194.8	97.40	48.70	32.47	24.35	19.48	16.23
6	1580.21	790.10	395.05	263.37	197.53	158.02	131.68
15	9056.44	4528.22	2264.11	1509.41	1132.06	905.64	754.70
20	15668.18	7834.09	3917.04	2611.36	1958.52	1566.82	1305.68
25	23970.27	11985.13	5992.57	3995.04	2996.28	2397.03	1997.52

From Table 5.24 and Table 5.25 can be seen that if the large current paths were to be implemented using on PCB surface, copper planes would have to be used due to maximum trace width being 250 mils in Mentor PADS. Current paths were instead chosen

to be implemented using silicon clad temperature resistant hookup wire, ring terminals and bus bars. One end of the hookup wires were planned to be soldered directly to the leads sourcing and sinking the current. The other ends are crimped to high temperature tolerant ring tongues and clamped to bus bars using M4 sized screws and screw connection terminals.

Hookup wire was selected to be either Helukabel SiHF or LappKabel ÖLFLEX® HEAT 180. Hookup wire from Helukabel can be used at 100% load value up to 150 ºC [51]. ÖLFLEX® HEAT 180 can be used at 100% load value up to 150 ºC [52] according to catalogue based on 2003 version of DIN VDE 0298-4 [53] or at 100% load value at least up to 130 ºC [54] according to catalogue based on 2013 version of DIN VDE 0298-4 [55].

Access to DIN VDE 0298-4 is restricted so Table 12-1 of LappKabels technical table document was used in the cable diameter selection [54]. According to the table mentioned previously, in case of single core cables, 2.5 mm^2 cross section cable has a nominal current rating of 32 Amps and a cable with 4 mm^2 cross section has a nominal current rating of 42 Amps. 4 mm^2 cross section cable was chosen to provide the current path from through hole mounted component leads to the screw connectors in order to account for possible load current de-rating due to cables being in close proximity to one another. 2.5 mm^2 cross section cable was chosen to provide high current paths from surface mounted component leads to the screw connectors due to 4 mm^2 cross section cable not fitting between the components on the designed PCB. Due to cables from outside the measurement board being 5 metres long 6 mm^2 cross section cable was chosen instead of 4 mm^2 cross section cable in order to reduce voltage drop in the by reducing the resistance of the wire. The resistance of the wire is inversely proportional to the cross sectional area according to Pouillet's law.

Semiconductor measurement board was designed to contain the tested components, bus bars and interface connectors. In order to provide off-state voltages and receive measurement signals 37-pole sub miniature connectors with temperature ranges of -55 ºC to 150 ºC were selected [56][57]. The design of sizing of bus bars was not finalized in the design used for this thesis. The pitch of the screw holes was however selected to be 14.30 mm and the diameter of the holes in the bus bar to be 5 mm in order to ease the mounting of M4 screw terminals. The components were designed to be screwed to a frame surrounding the measurement board which in turn would be mounted on a large heat sink. The details of frame and heat sink were not planned by the thesis writer and would require cooperation with a mechanical engineer. Estimations of wiring of the measurement board is illustrated in Figure 5.8 and references of the connections in figure are defined in Table 5.26. One of the goals of the small-scale prototype version was to test if the series connectors were accessible by hand with such a high amount of wiring with the series connections being in close proximities to one another. Due to the high temperature during

the thermal cycling test a PCB material with extended glass transition temperature was planned to be used. The main design priorities of the measurement semiconductor board was high temperature tolerance, capability to change the component series and parallel connections. The design schematics, layouts and drawings for the full-scale measurement board are in APPENDIX A.

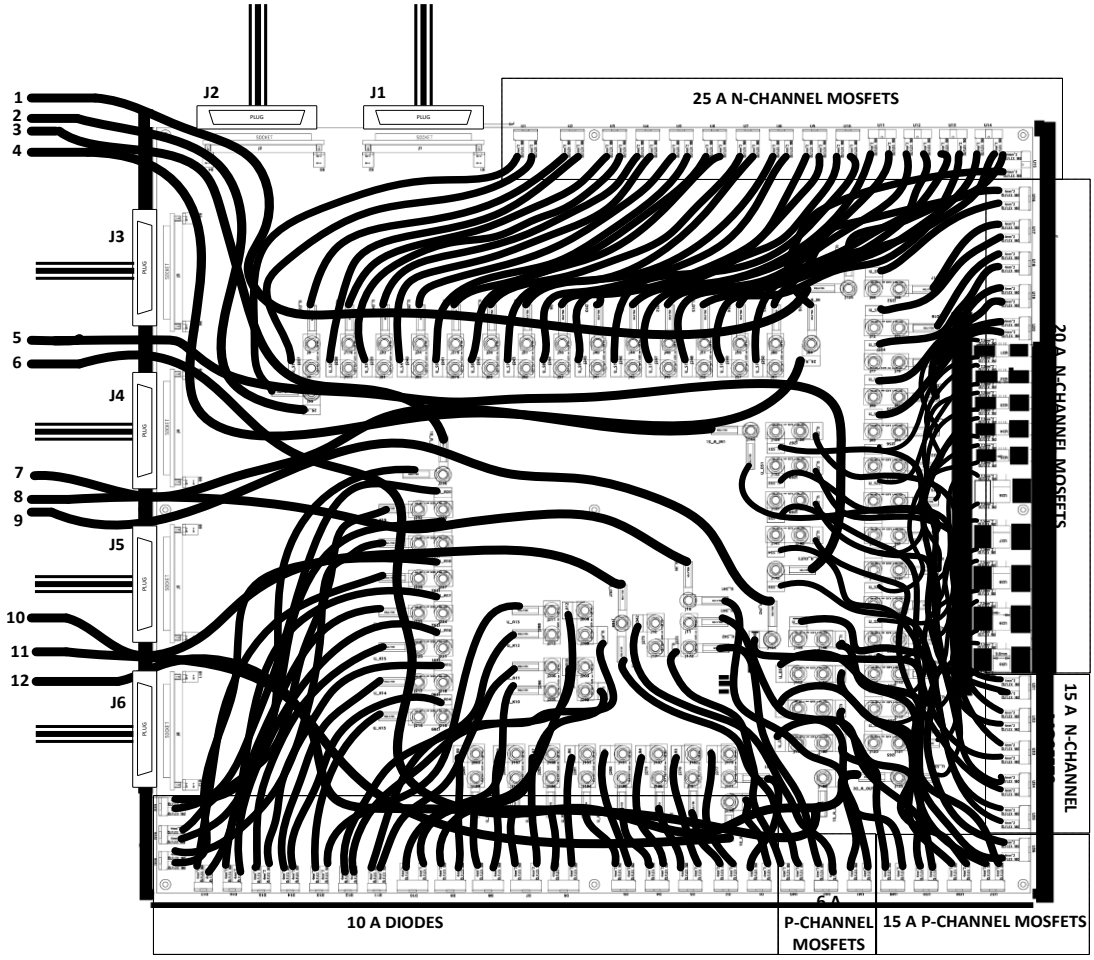


Figure 5.8 Estimated wiring of the semiconductor measurement board

Table 5.26 Reference designators of Figure 5.8

Ref-Des	Single core A(mm^2)	Number of Wires	Purpose
1	6	1	20A input to 20A MOSFETS
2	6	1	25A input to 25A MOSFETS
3	6	1	10A output from diodes
4	6	1	25A output from 25A MOSFETS
5	6	1	15A output from 15A N-Channel MOSFETS
6	6	1	20A output from 20A MOSFETS
7	6	1	15A input to 15A N-Channel MOSFETS
8	6	1	6A input to 6A P-Channel MOSFETS
9	6	1	15A input to 15A P-Channel MOSFETS
10	6	1	6A output from 6A P-Channel MOSFETS
11	6	1	15A output from 15A P-Channel MOSFETS
12	6	1	10A output to diodes
J1	0,5	37	Drain voltages from transistors U1-U35; Source voltages from transistors U36-U37
J2	0,5	37	Source voltages from transistors U38-U43; Source voltages from transistors U1-U28
J3	0,5	37	Source voltages from transistors U29-U35; Drain voltages from transistors U36-U43; Gate control and measurement voltages for transistors U1-U9; Gate control voltage for transistor U10
J4	0,5	37	Gate measurement voltage from transistor U10; Gate control and measurement voltages for transistors U11-U28
J5	0,5	37	Gate control and measurement voltages for transistors U29-U43; Anode voltages for diodes D1-D5
J6	0,5	37	Anode voltages for diodes D6-D20; Cathode voltages for diodes D1-D20

Break out box was designed to operate as a measurement, control voltage and open-state voltage interface for the other parts of the test setup. The surface of the box would contain 20-pin connectors for the 20 channel data aggregator, 37-pin D-sub miniature connectors for the interface with breakout box, 64-pin and 24-pin connectors for the MOSFET gate control board, banana sockets for the power supplies and ground references and buttons for individual component disconnection from the high voltage power supply. Single pole switches to short drain and source terminals of MOSFETs were also designed to be placed on the breakout box surface. To measure leakage current during the states when MOSFETs would have been reverse biased leakage measurement series resistors of 10 kΩ were planned to be used on the supply voltage side (high side) of the devices under tests. Additionally for diode types which had large leakage current variation according to

datasheets (D1-D16) [44][45][46], jumpers and external connections to high power leakage resistors were designed to be provided. Simplified operational diagram of the breakout box is illustrated in Figure 5.9. Reference designators for Figure 5.9 are defined in Table 5.27.

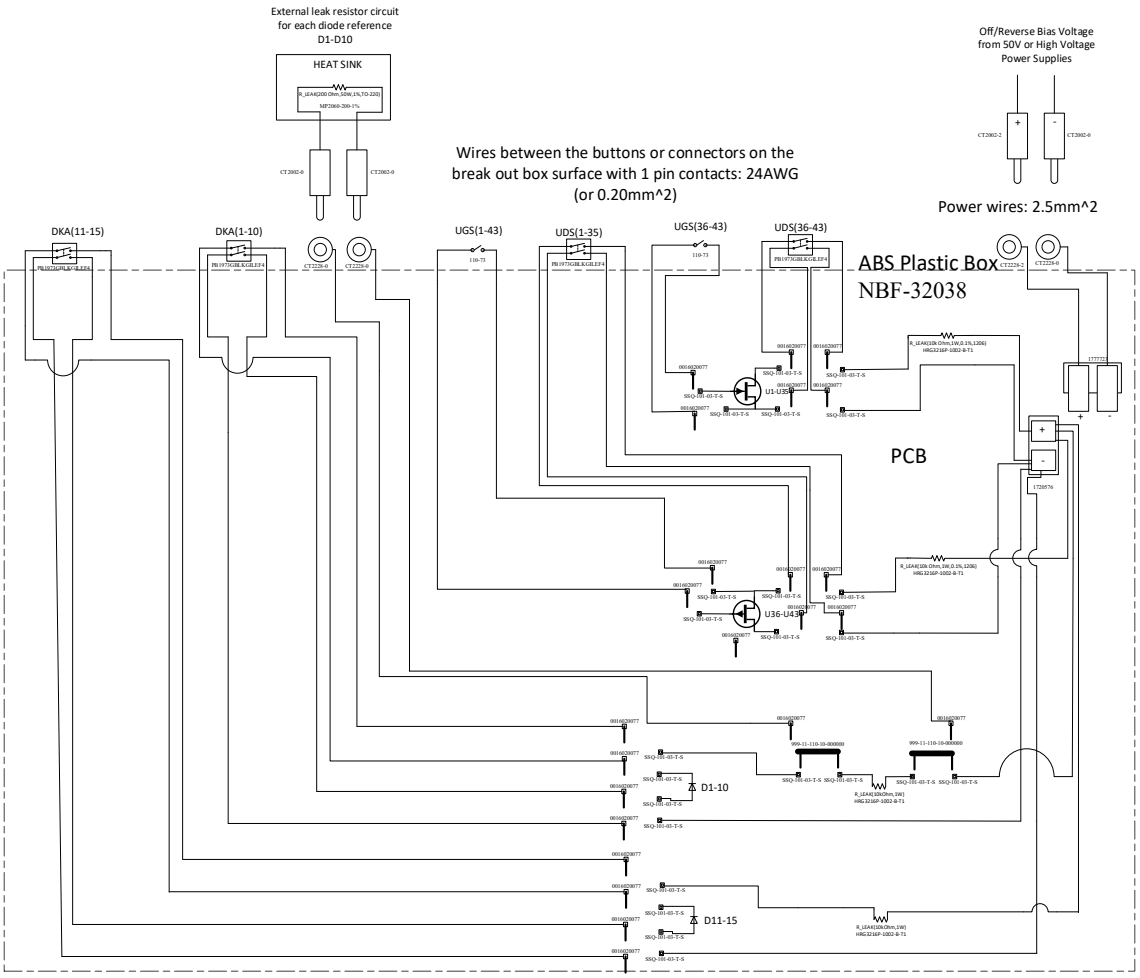


Figure 5.9 Simplified operational diagram of the breakout box

Table 5.27 Reference designators for Figure 5.9

Part Name	Description
1720576	2 Position Vertical Terminal Block Header, pitch 7.62mm
1777723	2 Position Terminal Block Plug, Female Sockets 0.300", (7.62mm) 180° Free Hanging (In-Line)
CT2002-0	Banana Plug Connector, Standard, Solder, Black
CT2002-2	Banana Plug Connector, Standard, Solder, Red
CT2228-0	Banana Jack Connector, Standard, Solder, Black
CT2228-2	Banana Jack Connector, Standard, Solder, Red
PB1973GBLKGILEF4	Pushbutton Switch DPST Standard, Illuminated Panel Mount, Snap-In
110-73	Toggle Switch, SPST, Panel Mount
0016020077	Pin Contact, Gold, 24-30 AWG, Crimp
SSQ-101-03-T-S	1 Position Receptacle Connector, Through Hole Tin
999-11-110-10-000000	2 (1 x 2) Position Shunt Connector, Non-Insulated, 0.100" (2.54mm), Gold

The main design priorities of the breakout box design were the simplicity of the electrical circuit, budget and ease of use. Schematics, layouts and mechanical sketches for the full-scale system version of the breakout box are in APPENDIX B.

MOSFET gate control board was designed to keep the tested transistors in saturation and provide constant Gate-to-Source voltages for each of the MOSFETs. The constant voltage is achieved in case of n-channel MOSFETs by summing amplifier configuration and in case of p-channel MOSFETs by differential amplifier configuration. Additional compensation and protection circuitry was added based on the Gate-to-Source voltage waveforms obtained by PSpice simulations. N-channel MOSFET Gate-to-Source voltage circuit is illustrated in Figure 5.10, P-channel MOSFET Gate-to-Source voltage circuit is in Figure 5.11 and reference voltage circuit is in Figure 5.12. R_wire resistors represent the estimated resistances of the wire connections. In the voltage reference circuit the reference voltage was designed to be adjusted using a 50 kΩ potentiometer. Time controlled switches in Figure 5.12 represent turning the potentiometer to maximum and minimum values. The Zener diode in the voltage reference circuit was designed to clamp the maximum reference voltage to 13V.

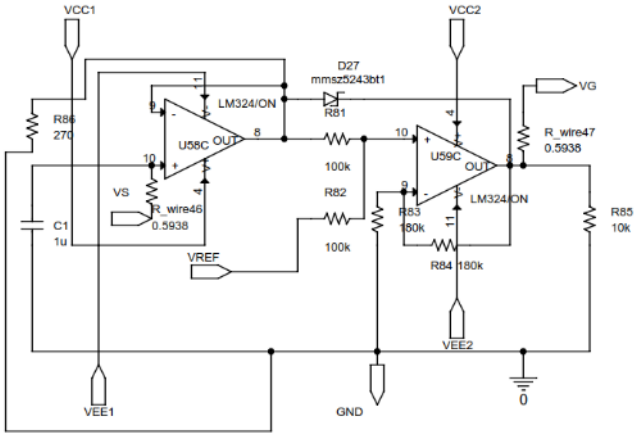


Figure 5.10 N-channel MOSFET Gate-to-Source voltage circuit

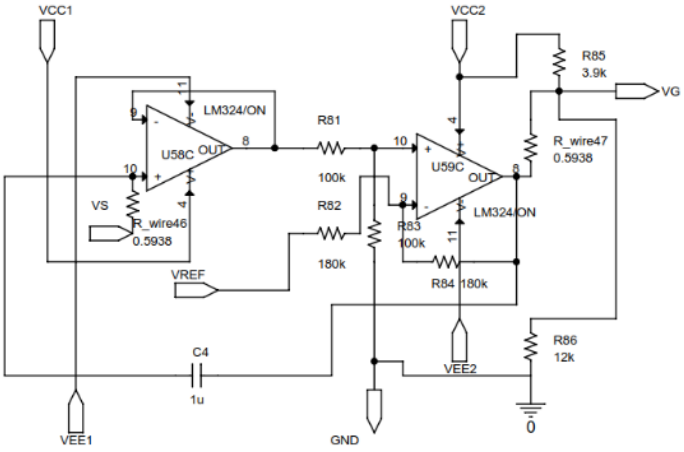


Figure 5.11 P-channel MOSFET Gate-to-Source voltage circuit

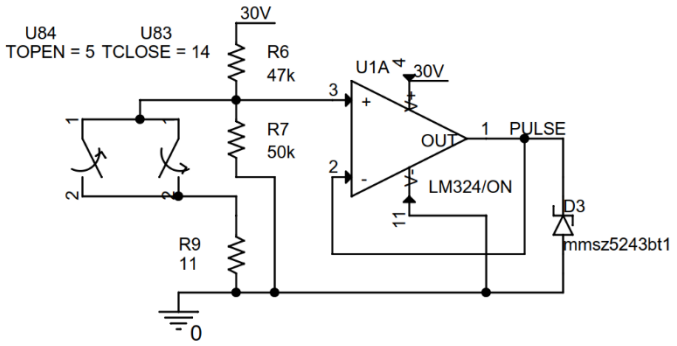


Figure 5.12 Reference voltage for the Gate-to-Source circuits

In case of n-channel MOSFET Gate-to-Source voltage circuit Zener diode and 270 Ohm resistors are designed to clamp voltage spikes in gate voltage output. Capacitor between non-inverting input of the voltage follower increases stability in the event the reference

voltage is low judging by simulations. 10 kΩ resistor is designed to pull the gate voltage to ground in case the operation amplifiers are not powered. Output from the summing stage of the n-channel MOSFET Gate-to-Source voltage circuit would be the sum of VS and VREF in a case where resistors would be ideally matched to the values in circuit.

In the p-channel MOSFET Gate-to-Source voltage circuit the capacitor between non-inverting input of the voltage follower and the output of the differential amplifier contributes to stability according to simulations. 3.9 kΩ and 12 kΩ resistors in the differential amplifier output are designed to bias the gate voltage of the p-channel MOSFET to 15 V in the event the operational amplifier was not powered. If the operational amplifier was not powered and the test voltage would be 15 V, Gate-to-Source voltage would be zero Volts. Drain-to-Source on resistances and threshold voltages of the MOSFETs in the full-scale tests are defined in Table 5.28 and used to calculate the minimum and maximum voltage requirements for the MOSFET gate control circuit outputs. The required gate voltages in respect to ground can be estimated in worst case scenario based on the Drain-to-Source voltages in the series connections in Table 5.22. The total voltage drops in the series connections are defined in Table 5.29.

Table 5.28 Maximum on-resistances and minimum threshold voltages of the MOSFETs

Ref-Des	Model	R_{DSOn_max}(Ω) at T_J = 150 °C	V_{GSTh_min}(V)
U1-U5	IRHMS57160[37]	0.028	2
U6-U10	JANSR2N7470T1[37]	0.01216	2
U11-U15	SCTW100N65G2AG[43]	0.023	1.9
U16-U20	STRH100N10HY1[35]	0.066	1.5
U21-U25	SQJ402EP[41]	0.36	1.5
U26-U30	FDB3652_FO85[42]	0.0414	2
U31-U35	IRHMS67260[38]	0.06526	2
U36-U40	STRH40P10HY1[36]	0.126	-2
U41-U43	2N7236[40]	0.36	-2

Table 5.29 Total voltage drops in MOSFET series connections in the test

Series Connection Ref-Des	I_{TEST}(A)	Total Voltage Drop due to R_{DSOn}(V)
A	25	7.90
B	20	12.84
C	15	14.34
D	6	8.64

The voltage drop in case of p-channel transistors in series connection C would be larger than in the case of D due to larger number of the series connected transistors. Thus, U40

would have the most negative voltage in reference to ground compared to other transistors. Required gate voltage for U40 can be calculated with the following equations:

$$V_{TEST} = 15\ V;\ I_{TEST} = 15\ A; R_{DSOnmax(STRH40P10H1)} = \ 0.126\ \Omega \quad (15)$$

$$V_{S(U40)} = V_{TEST} - 4\ I_{TEST} R_{DSOnmax(STRH40P10H1)}, \quad (16)$$

$$V_{G(U40)} = V_{S(U40)} - V_{REF}, \quad (17)$$

$$If V_{REF} = 12\ V\ then\ V_{G(U16)} = -4.56\ V, \quad (18)$$

where V_{TEST} is the voltage of the high current power supply during the test, I_{TEST} is the current in the series connection, R_{DSOn} is the Drain-to-Source on-resistance, V_{REF} is the Gate-to-Source reference voltage and V_G is the gate voltage.

Uppermost transistor in series connection B has the largest gate voltage requirement due to voltage drop being larger than in series connection A. The required gate voltage for U16 can be calculated with the following equations:

$$V_{TEST} = 15\ V;\ I_{TEST} = 20\ A; R_{DSOnmax(STRH100N10HY1)} = \ 0.066\ \Omega \quad (19)$$

$$R_{DSOnmax(SSQJ402EP)} = \ 0.021\ \Omega; R_{DSOnmax(FDB3652\_FO85)} = \ 0.0414\ \Omega \quad (20)$$

$$V_{DROP1} = 4R_{DSOnmax(STRH100N10HY1)}\ I_{TEST} \quad (21)$$

$$V_{DROP2} = 5R_{DSOnmax(STRH100N10HY1)}\ I_{TEST} \quad (22)$$

$$V_{DROP3} = 5R_{DSOnmax(STRH100N10HY1)}\ I_{TEST} \quad (23)$$

$$V_{S(U16)} = V_{DROP1} + V_{DROP2} + V_{DROP3}, \quad (24)$$

$$V_{G(U16)} = V_{S(U16)} + V_{REF}, \quad (25)$$

$$If V_{REF} = 12\ V\ then\ V_{G(U16)} = 23.52\ V, \quad (26)$$

In order to ensure that the transistors are in cut-off state, the control circuit is required to provide Gate-to-Source voltage that is less than the minimum threshold voltage of the MOSFETs. Minimum gate voltage for the n-channel MOSFET control circuit should thus be less than 1.5 V. P-channel MOSFET maximum gate output should be at least two Volts below the test voltage in order to ensure that tested MOSFETs are in cut-off state.

Voltage slew rate and bandwidth were not considered priorities in the design due to MOSFETs needing only constant voltage throughout the testing phase. LM324 was chosen as the amplifier to drive the MOSFETs due to wide supply voltage range, large output swing, availability of simulation models and number of amplifier in a single integrated circuit [58]. LM324 is additionally cheap according to Farnell [59].

Simulations for the MOSFET gate control circuits can be found in APPENDIX C. Schematics, PCB layouts, assembly diagrams and drill diagrams can be found in APPENDIX D.

5.5 Summary

Several space grade MOSFETs, relays, diodes and two bypass switches were planned to be tested in order to assess the capability of the aforementioned components to perform the passivation functions. Three automotive grade MOSFET types and one automotive grade diode type were also planned to be added to the tests. The lengths of the tests for semiconductors and relays were estimated using Norris-Landzberg and Arrhenius equations using predefined satellite field conditions. Tested components had varying electrical bias conditions depending on the simulated passivation function, power supply power, component ratings and tests. In order to optimize power consumption during tests several component types needed to be connected in series. Every passivation relevant parameter was planned to be measured in case of relays and semiconductors before and after the use of thermal chambers. During the tests with thermal chambers only the parameters relevant to then ongoing phases were planned to be measured. The switching of relays between the nominal mission phase and disposal phase was planned to be carefully monitored. For bypass switches only the switching voltage test was planned.

Test setup for the semiconductor was designed to power supplies, power distribution blocks, measurement channel adaptors, measurement equipment, a breakout box, MOSFET gate control board and measurement board that would be put in the thermal chamber. The measurement board would house the components planned to be tested and provided large current paths for the series connections of the components that would be in conducting state. Measurement data and off-state voltages were planned to be provided by using a breakout box as an interface. The box would also have the capability to disconnect and connect individual components from the high voltage power supply and short the gates and sources of individual transistors using buttons. Constant Gate-to-Source voltages would be provided for the MOSFETs using the MOSFET gate control board. Output voltage range for the circuits planned to drive n-channel and p-channel MOSFETs can be found in Table 5.30.

Table 5.30 MOSFET control board high and low output conditions

Signal	Low condition	High condition
p-MOSFET V_{GS}	$V_G < -4.56$ V	$V_G > V_{TEST} - 2$ V
n-MOSFET V_{GS}	$V_G < 1.5$ V	$V_G > 23.52$ V

The gates were planned to be driven using LM324 with protection circuits. The capacitors were selected based on transient simulations of the Gate-to-Source voltages in order to stabilize the circuits.

6 SMALL-SCALE SEMICONDUCTOR TEST SYSTEM

In order to assess the usability and operational principles of the full-scale test system a small-scale prototype was designed and tested. The prototype contained a breakout box, measurement board, MOSFET gate control card and two measurement channel selector boards. The system was designed on Tampere University of Technology premises. Equipment of TUTLab and Electronics and Communication department was used in assembly of the system. Layouts, assembly diagrams and schematics were designed using Mentor PADS. Design of cut outs and drill diagrams on the enclosures was designed using Solidworks 2017. The lid on the breakout box was 3D printed using TUTLab equipment. The 3D model of the lid was designed using Solidworks 2017.

In this chapter, the parts of the miniature test system are described. The measurements on the tested components are described and detailed. The design and implementation issues encountered during the production of the test system are also mentioned.

6.1 Components of the Small-scale Test System

A miniature version of the semiconductor test system was designed with fewer parts and different components. The block diagram of the designed test system is in Figure 6.6. In order to simulate 20-channel interface measurement the data logger was replaced with a measurement channel selector board. PCB clearance rules were as defined in the full-scale system design. The built system is in Figure 6.1. The main objectives in the creation of the miniature test system was to test if the MOSFET gate control board would perform within the desired parameters described in previous chapter and if the measurement data obtained with the system would correspond to the parameters described in datasheets of the tested components. Another concern was to test if the series connection manipulation was on the measurement board was possible and easy by hand.

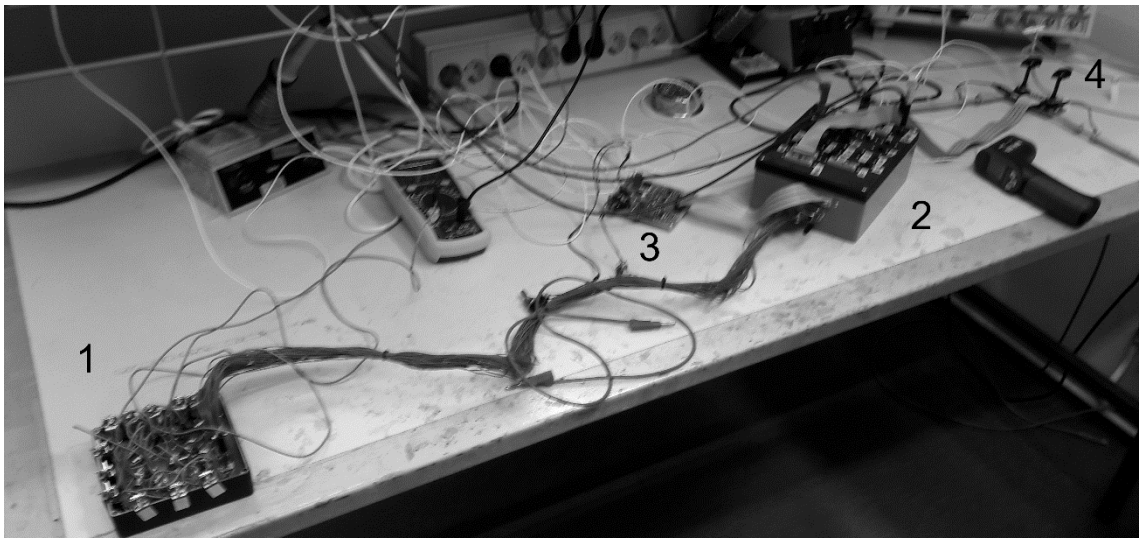


Figure 6.1 Miniature Test System. 1. Measurement board 2. Breakout box 3. MOSFET Gate Control Board 4. Oscilloscope Channel Selector

Three p-channel MOSFETs, three n-channel MOSFETs and five diodes were selected as the components on the measurement board. High current paths were implemented by soldering ÖLFLEX® HEAT 180 hook up wire with 0.50 mm^2 cross section to component leads. Ring tongue connector was crimped on the non-soldered ends of the hook up wire which was screwed on a brass terminal jumper in on top of M4 screw connector terminals in order to provide series connections. Packages chosen for the components for the tests were TO-220AB due to the mounting style to heatsinks being screw based.

MOSFETs were chosen based on price and Drain-to-Source on-resistances. The on-resistances were required to be in case of n-channel MOSFETs large enough to force gate voltage of the uppermost MOSFET to be over 15 Volts with the selected test current. In case of p-channel MOSFETs the On-resistance was planned to be sufficiently large to force the gate voltage of the lowermost MOSFET to be under 0 Volts. Diodes were chosen based on the assumption that the heating tab of the package not being electrically connected to any of the leads. The assumption was proven false in the assembly phase. A vertical 150 ºC tolerant 37-pole D-sub miniature connector was used as an interface to off-state voltages and measurement signal paths from the breakout box. The design documents for the miniature semiconductor measurement board are in APPENDIX E. The built semiconductor measurement board is in Figure 6.2.

Main objective in building of this board was to test if there was enough room to change the series connections on the board with similar pitch as the case of the full-scale system. Initially the heat transfer tabs TO-220AB were not assumed to be electrically connected to any of the leads. After tests it was discovered that the tabs were connected to the middle lead of the packages (drain for the MOSFETs and cathode for the diodes). Due to the electrical connections, anodized heatsinks were used as insulation between the tabs and

aluminium case and the devices were clamped to the walls of the aluminium enclosure instead of using the screw holes.

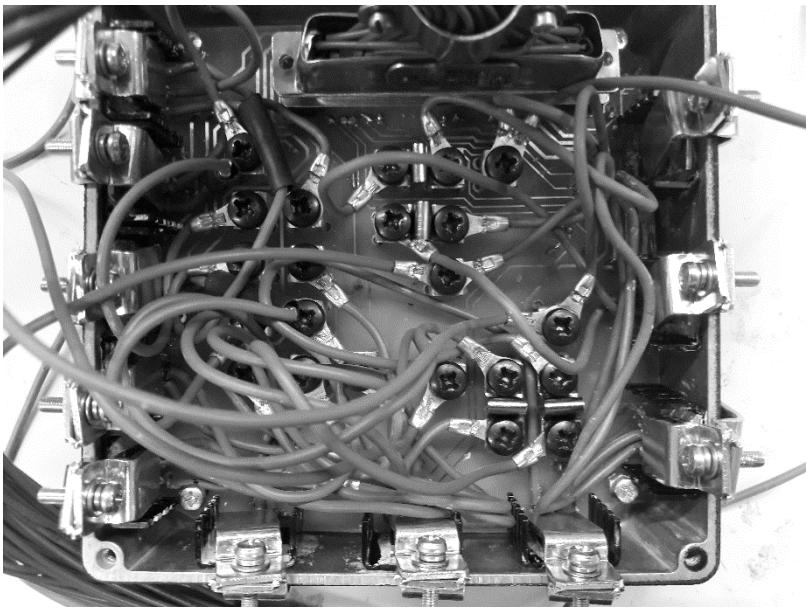


Figure 6.2 Miniature semiconductor measurement board with MOSFETs connected in series

Breakout box exterior provides an interface for measurement channel selector (20-pin connector), measurement board (37-pin D-sub miniature connector) and MOSFET gate control board (20 pin connector). Additionally the box has buttons to disconnect individual components from the open state voltage by using DPDT slide switches. Same slide switch type was used to provide the ability to short MOSFET gates to sources in order to ensure that Gate-to-Source voltages would be 0 V. The PCB inside breakout box contained the connectors to breakout box exterior in addition to leakage current measurement resistors. The resistors were chosen to be on high side in respect to the tested components. The resistances and power ratings of the resistors were chosen based on maximum and minimum leakage currents of the tested components. The design documents for the miniature breakout box are in APPENDIX F. Built breakout box is in Figure 6.3. Vertical switches connected and disconnected components from and to the 30 Volt power supply. Horizontal switches short and open the gate and source terminals of the tested MOSFETs. Vertical switches are open when the slider is in lower position and horizontal switches are open when the slider is in left position.

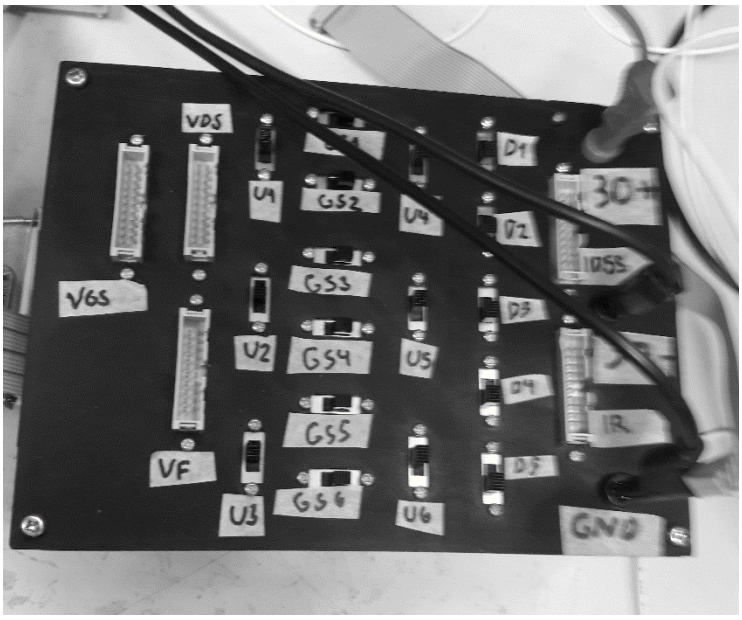


Figure 6.3 Miniature system breakout box

Miniature MOSFET gate control card mostly uses the same components and circuits as the full-scale version. Due to there being only six testable MOSFETs the number of needed LM324 was four. The interface was designed to use 20-pin connector instead of 64-pin and 24-pin versions. Unused amplifiers were pulled down by connecting the inverting inputs to the outputs and non-inverting outputs to ground potential. Additionally jumpers were provided in order to simulate loss of gate control voltages for some transistors of the test. The design documents for the miniature gate control board are in APPENDIX G. The constructed miniature MOSFET gate control board is in Figure 6.4.

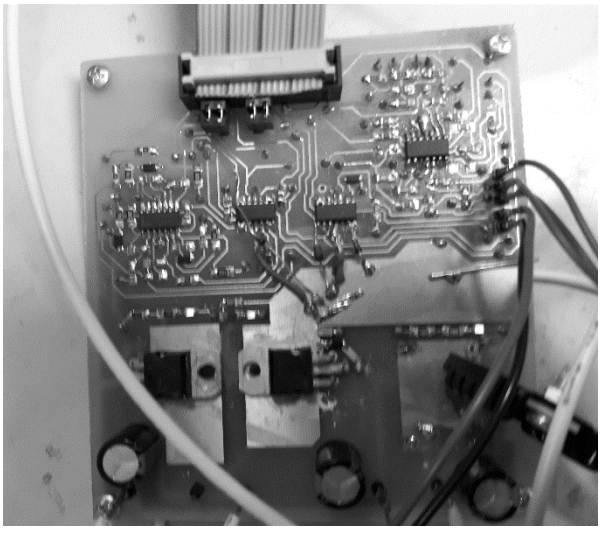


Figure 6.4 Miniature system MOSFET gate control board with additional protection circuitry and supply voltage changes based on tests.

The oscilloscope channel selector was designed to provide 20 channels for the two-channel oscilloscope using rotary switches. Oscilloscope probe was designed to be connected to the switch outputs (L and R) and using differential mode, 10 differential measurements would be possible. Additionally each of the measurement channels was designed to have an additional pin header connector for debugging purposes. The design documents for the oscilloscope channel selector are in APPENDIX H. The Oscilloscope channel selector is in Figure 6.5. Measurement channels are selected by rotating the knobs. For a single differential measurement the knobs must point at the same channel. The engraved switch position indicators on the rotary switches were used as the channel indicators.

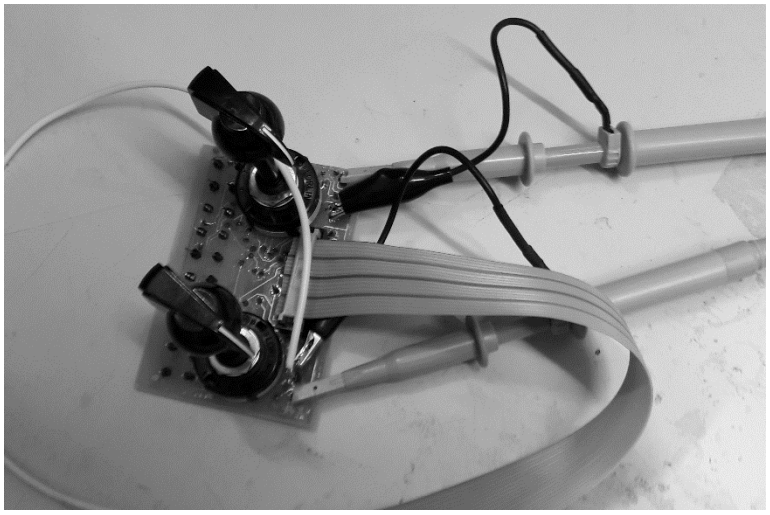


Figure 6.5 Oscilloscope channel selector

Miniature test system had to be modified after construction due to the design faults and mistakes made during the design, manufacturing and assembly. Several shorts and open circuits were initially present due to mistakes made during development and etching of the boards. P-channel MOSFET driving operational amplifier was damaged and replaced several times during tests in particular.

6.2 Small-scale test system measurements

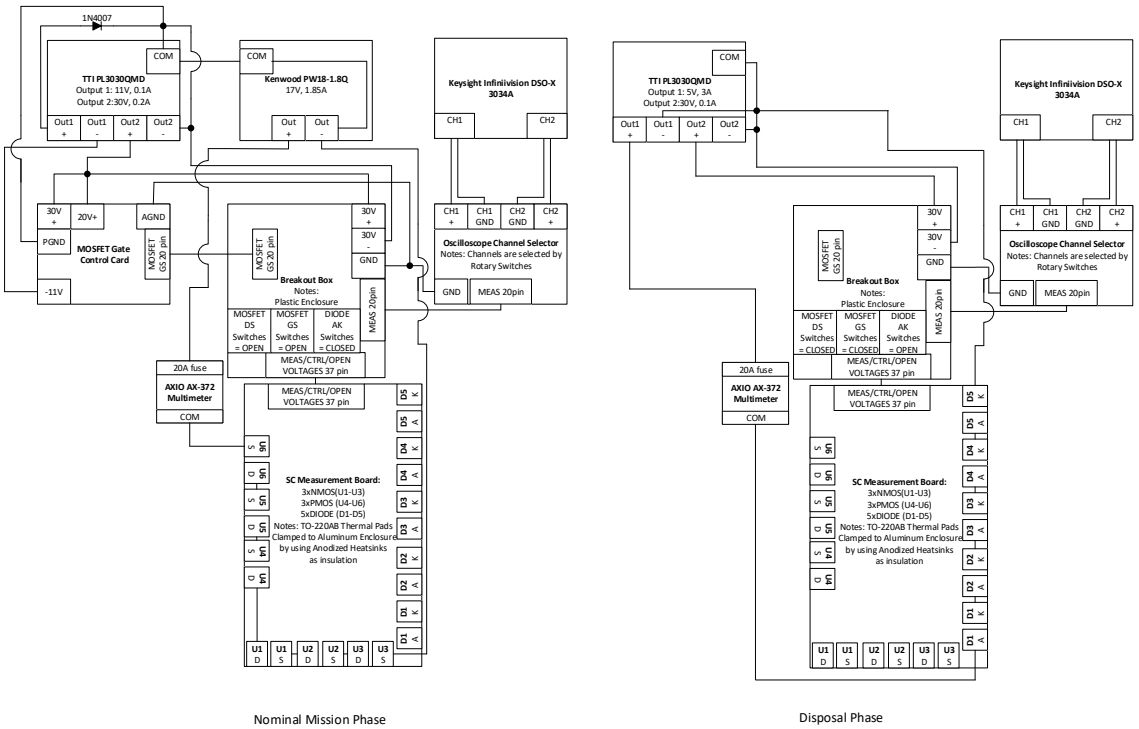
The small-scale test system measurements were performed in in two phases for all the components. In addition, a threshold voltage measurements was performed for each MOSFET. In the first phase, which corresponded to the nominal mission phase, all the MOSFETs were connected in series and diodes reverse biased. Passivation relevant parameters of the MOSFETs selected for testing are in Table 6.1. Passivation relevant parameters of the diodes selected for testing are in Table 6.2. Block diagram of the test setup is in Figure 6.6. Assumed bias conditions for the components in test are in Table 6.3.

Table 6.1 Datasheet parameters of the MOSFETs selected for testing

Ref-Des	Model	V_{DSmax} (V)	I_{DS} max (A)	R_{DSOn} max (Ω)	I_{DSS} max (μA)	V_{GSTh} min (V)	V_{GSTh} max (V)
U1	IRF610PBF 100[60]	200	2.1	1.5	250	2	4
U2	IRF610PBF	200	2.1	1.5	250	2	4
U3	IRF610PBF	200	2.1	1.5	250	2	4
U4	IRF9630PBF [61]	-200	-4	0.8	-500	-2	-4
U5	IRF9630PBF	-200	-4	0.8	-500	-2	-4
U6	IRF9630PBF	-200	-4	0.8	-500	-2	-4

Table 6.2 Datasheet parameters of the diodes selected for testing

Ref-Des	Model	V_R max (V)	I_F max(A)	V_F typ@3A (V)	V_F max@3A (V)	I_R max (mA)
D1	FERD30M45CT[62]	45	15x2	0.25	0.35	50
D2	FERD30M45CT	45	15x2	0.25	0.35	50
D3	FERD30M45CT	45	15x2	0.25	0.35	50
D4	FERD30M45CT	45	15x2	0.25	0.35	50
D5	FERD30M45CT	45	15x2	0.25	0.35	50



Nominal Mission Phase

Disposal Phase

Figure 6.6 Block diagram of the test setup

Table 6.3 Bias condition assumptions for the test setup

Type	**Model**	**Nominal Mission Phase**		**Disposal Phase**	
MOSFET	IRF610PBF	V_{ON} = 17 V V_{DS} = 2,78 V	I_{DS} =1.85 A	V_{OFF} = 30 V V_{DS} = 30 V	I_{DS} = 0 A
	IRF9630PBF	V_{ON} = 17 V V_{DS} = -1.48 V	I_{DS} = -1.85 A	V_{OFF} = 30 V V_{DS} = -30 V	I_{DS} = 0 A
Diode	FERD30M45 CT	V_R = 30 V	I_F = 0 A	V_{ON} = 1.75 V V_F = 0.35 V	I_F = 3 A
V_{GS}(n-MOSFET)		12V		0V	
V_{GS}(p-MOSFET)		-12V		0V	

During the nominal mission phase MOSFET Drain-to-Source voltages, MOSFET Gate-to-Source voltages, diode leakage-resistor voltages and MOSFET on-state current measurements were performed. Additionally case temperatures were measured using infrared thermometer. Initially when MOSFETs were turned on, the voltage across the series connection was nine Volts with 1.85 A current passing through. Several minutes after the start of the measurements voltage rose to 17 V and current dropped to 1.69 A. The change of the voltage and current across the MOSFET series connection is assumed to have happened due to Drain-to-Source on-resistance increase caused by the risen junction temperatures. Power supply electrical bias conditions in the nominal mission phase are in Table 6.4. MOSFET Drain-to-Source voltage measurements, peak to peak voltage variation during the measurement, current measurement and Drain-to-Source On-resistances were calculated by division of measured Drain-to-Source voltages by the measured Drain-to-Source currents. Calculations based on the aforementioned measurements are in Table 6.5.

Table 6.4 Measured power supply bias conditions during nominal mission phase

Power Supply	**I_{LIMIT}(A)**	**V_{LIMIT}(V)**	**$I_{MEASURED}$(A)**	**$V_{MEASURED}$(V)**
PL3030QMD Channel 1	0.1	11	0.020	11.10
PL3030QMD Channel 2	0.2	30	0.054 (0.130 when driving MOSFETs with maximum V_{GS})	30.01
PW18-1.8Q	1.85	17	Initial: 1.85 Stabilized: 1.69	Initial: 9 Stabilized: 17

Table 6.5 R_{DSOn} measurement of MOSFETs

Ref-Des	I_{DS}(A)*	V_{DS}(V)	V_{PP}(V)**	T_{case}(°C)	R_{DSOn}(Ω)
U1	1.73	5.41	0.04	60.9	3.13
U2	1.71	3.31	0.04	48.7	1.94
U3	1.71	2.97	0.04	41.8	1.73
U4	-1.71	-1.54	0.05	63.2	0.90
U5	-1.70	-1.53	0.05	56	0.90
U6	-1.69	-1.55	0.05	53.2	0.92

* The current was slowly decreasing throughout the measurement presumably because of the increase of transistor on-resistance due to heating.

**Peak to peak variation is small compared to the measured values so error analysis was not performed in the case of these measurements

Calculated resistances exceed the maximum Drain-to-Source On-resistances found in the datasheets of the devices [60][61]. The datasheets state that the provided parameters were valid when junction temperature was 25 °C. Drain-to-Source on-resistance multipliers based on the junction temperatures can be found in the datasheets of the MOSFETs. The circuit in Figure 6.7 can be used to estimate the channel (junction) temperature [63]. By using Ohms law with dissipated power as current and thermal resistance as resistance, the equivalent circuit the junction temperature can be estimated as the sum of case temperature and the product of caste temperature and channel to package (junction-to-case) thermal resistance. Junction temperature calculations based on the circuit are in Table 6.6.

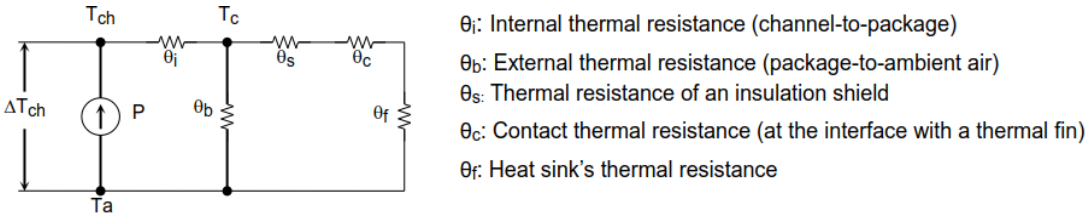


Figure 6.7 Thermal radiation steady state equivalent circuit [63]

Table 6.6 Corrections based on junction temperature vs normalized R_{DSOn} graphs

Ref-Des	$R_{thJCmax}$ (°C/W)	P_D* (W)	T_C(°C) **	T_J (°C) ***	$R_{DSOn@TJ}$ multiplier	$R_{DSOnmax}$ (Ω)
U1	3.5 [60]	3.13	60.9	71.8	1.4 [60]	2.1
U2	3.5	1.94	48.7	55.5	1.3 [60]	1.95
U3	3.5	1.73	41.8	47.9	1.25 [60]	1.875
U4	1.7 [61]	0.90	63.2	64.7	1.3 [61]	1.04
U5	1.7	0.90	56	57.5	1.25 [61]	1
U6	1.7	0.92	53.2	54.7	1.25 [61]	1

* Calculated using $P_D = V_{DS} * I_{DS}$

** Case temperature

*** Junction temperature

After the maximum allowable Drain-to-Source on-resistances were corrected based on the junction temperatures, all measured on-resistances fit below the maximum values with the exception of U1. Possible causes for the discrepancy could be bad case temperature measurement or reasons internal to the MOSFET. Measured on-resistance of U1 would be within the maximum values if the junction temperature was over 130 °C (110 °C case temperature).

Diode leakage current was obtained by dividing the measured voltage over leakage measurement resistors by the resistances of the resistors. The measured values and leakage current calculations are in Table 6.7.

Table 6.7 Diode leakage current measurements

Ref-Des	V_{LEAK}(V)	V_{PP}(V)	R_{LEAK}(Ω)	I_R(mA)	I_{Error}(mA)	T_C(°C)
D1	0.3383	0.34	99.6	3.4	±1.7	68.5
D2	0.3104	0.34	99.6	3.1	±1.7	53.5
D3	0.3185	0.34	99.6	3.2	±1.7	37.7
D4	0.2145	0.34	99.5	2.2	±1.7	47.5
D5	0.2153	0.34	99.2	2.2	±1.7	28.9

Measured leakage current is within minimum and maximum values specified in Table 6.2. Leakage current resistors were placed on the high side compared to the tested components. This limited the resolution of the measurement peak-to-peak voltages. In order to reduce the problem, the breakout box must be redesigned by placing the leakage current measurement resistors on the low side (between the component in test and ground) compared to the components under test.

In the conditions simulating the disposal phase, MOSFET gate control board and the second power supply were removed from the system as illustrated in Figure 6.6. Diodes were disconnected from the 30V supply by the D1-D5 switches on the breakout box and

connected in series using the brass jumpers that were removed from MOSFET series connection. MOSFETs were connected to the 30V power supply using setting U1-U6 switches in the upper position. The gates of MOSFETs were shorted to sources using GS1-GS6 switches. Power supply electrical bias conditions in the disposal phase are in Table 6.8.

Table 6.8 Measured power supply bias conditions during disposal phase

Power Supply	I_{LIMIT}(A)	V_{LIMIT}(V)	$I_{MEASURED}$(A)	$V_{MEASURED}$(V)
PL3030QMD Channel 1	3	5	3.004	1.85
PL3030QMD Channel 2	0.1	30	0.021	30

MOSFET Zero-Gate-Voltage-Drain-Current was obtained by dividing the measured voltage over the measurement resistors by the resistances of the resistors. The measured parameters are in Table 6.9.

Table 6.9 MOSFET Zero-Gate-Voltage-Drain-Current measurements.

R_{LEAK}(Ω)	V_{LEAK}(V)	V_{PP}(V)	I_{DSS}(µA)	I_{Error}(µA)	T_C(°C)
178400	0.8242	0.8	4.62	±2.24	23.8
177500	0.8237	0.8	4.64	±2.25	23.7
178400	0.8272	0.6	4.64	±1.68	27.1
81700	0.2103	0.6	-2.57	±3.67	28.4
81800	0.2079	0.6	-2.54	±3.67	32.7
81700	0.2092	0.6	-2.56	±3.67	30.7

In the Zero-Gate-Voltage-Drain-Current measurements, the resistors were placed on high side compared to the tested MOSFETs. The lack of measurement resolution caused peak-to-peak voltage to be very large portion of the measured values. In the case of p-channel MOSFETs, the current measurement the peak-to-peak variation was larger than the voltage measured over the leakage resistor. As the case with diodes, the leakage current resistors should be placed on the low side of the components in order to allow more accurate measurement channel selection from the oscilloscope. If the average of the measured voltages was to be used, the Zero-Gate-Voltage-Drain-Current currents were within the maximum limits defined in Table 6.1.

Diode forward voltage measurement from the series connection did not require any additional calculations. The measured values can be found in Table 6.10

Table 6.10 Diode forward voltage measurements

Ref-Des	I_F(A)	V_F(V)	V_{PP}(V)	T_C(°C)
D1	3.004	0.248	0.03	32.4
D2	3.004	0.2434	0.03	27.7
D3	3.004	0.2518	0.03	26.2
D4	3.004	0.2528	0.03	25.4
D5	3.004	0.2508	0.03	25.4

The measured forward voltages were within or below the typical values defined in Table 6.2. The temperature rise of components in disposal phase was small in comparison to nominal mission phase.

In addition to measurements done in nominal mission and disposal phases of the test MOSFET threshold voltages and Gate-to-Source voltage startup waveforms were measured. Maximum outputs of the MOSFET gate control card were also tested.

In order to measure the threshold voltage, a copy of oscilloscope channel selector had to be manufactured. One channel selector was connected to the Gate-to-Source voltage measurement pins on the breakout box and one channel selector was connected to Drain-to-Source voltage pins on the breakout box. The connections in the system were similar to nominal mission phase. Instead of series connection, however Individual MOSFETs were connected to the PW18-1.8Q power supply with bias properties defined in Table 6.11. In case of n-channel MOSFETs the sources of individual transistors were connected to PW18-1.8Q negative pole and drain to PW18-1.8Q positive pole. Drain and gate voltages were monitored as gate voltage was steadily increased. The threshold voltage was obtained from the gate voltage when the transistor began conducting. In case of p-channel MOSFET the source of the transistor was connected to the positive pole and drain to the negative pole instead. The threshold voltage was obtained by subtracting the gate voltage from source voltage once the transistor began conducting. Threshold voltage measurement waveforms can be found in APPENDIX I. Measured threshold voltages can be found in Table 6.12.

Table 6.11 V_{GSTh} measurement power supply bias

Power Supply	I_{LIMIT}(A)	V_{LIMIT}(V)
PL3030QMD Channel 1	0.1	11
PL3030QMD Channel 2	0.2	30
PW18-1.8Q	0.003	6 (7 for U6 due to the output being damaged)

Table 6.12 Measured threshold voltages.

Ref-Des	V_{GSTh}(V)	V_{PP}(V) (from VGS measurements)	V_{ERROR}(V)
U1	4.16	0.2	0.1
U2	4.05	0.24	0.12
U3	4.15	0.24	0.12
U4	-3.779	0.05	0.025
U5	-3.802	0.05	0.025
U6	-3.761	0.06	0.03

The measurement threshold voltages of U1 and U3 are slightly above the maximum threshold voltages defined in Table 6.1. Other transistor threshold voltages are within the specified limits. The discrepancy of the values in case of U1 and U2 from the datasheet values can possibly be caused by inaccuracies produced by the measurement setup or internal parameters of the measured MOSFETs.

Startup Gate-to-Source voltages were plotted from the same bias configuration as in nominal mission phase. The objective was to observe if any of the Gate-to-Source voltages would have spikes over 15 V, which is the de-rated maximum Gate-to-Source voltage limits of transistors in the tests of the full-scale system. Gate-to-Source wave forms for U1, U2, U3, U4, U5 and U6 can be found in Figure 6.8, Figure 6.9, Figure 6.10, Figure 6.11, Figure 6.12 and Figure 6.13. The waveforms were obtained by turning the 50 kΩ from minimum value to maximum value and back to minimum value.

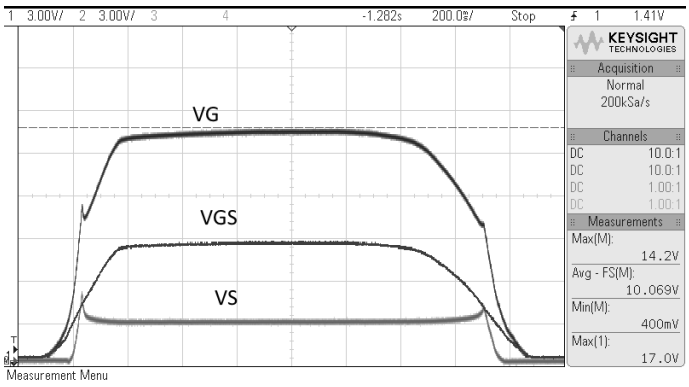


Figure 6.8 Gate-to-Source voltage of U1

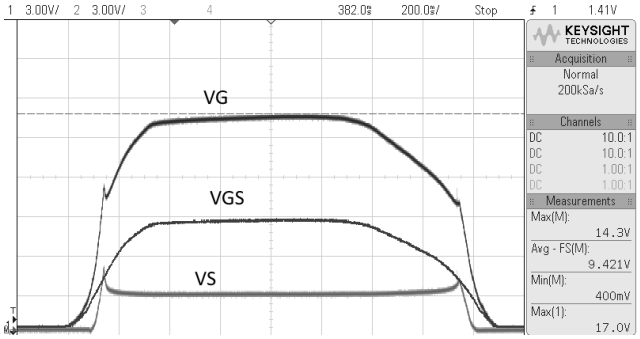


Figure 6.9 Gate-to-Source voltage of U2

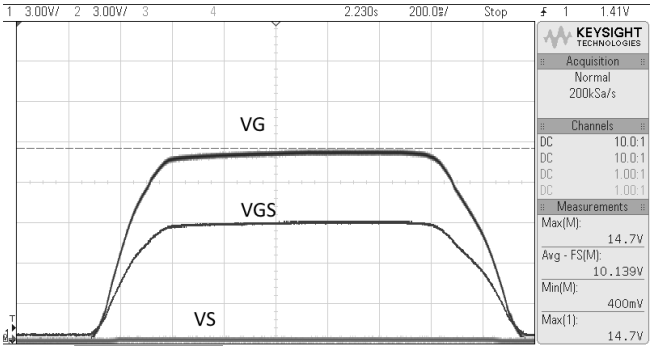


Figure 6.10 Gate-to-Source voltage of U3

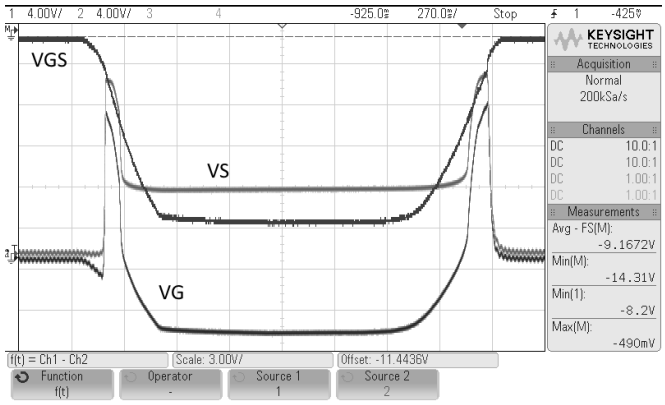


Figure 6.11 Gate-to-Source voltage of U4

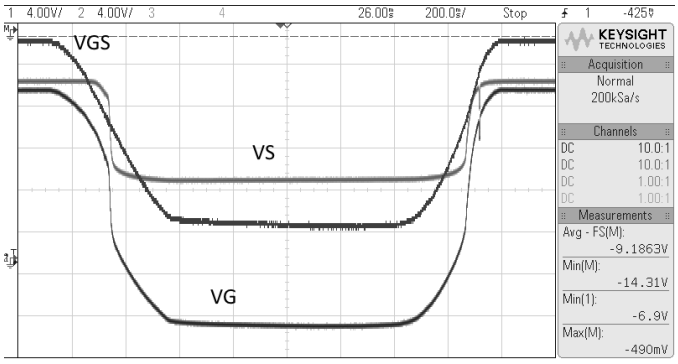


Figure 6.12 Gate-to-Source voltage of U5

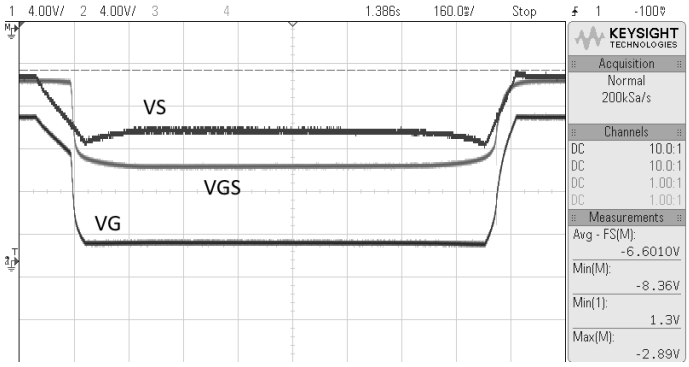


Figure 6.13 Gate-to-Source voltage of U6.

After modifying the MOSFET gate control card as described in Chapter 6.3 the output waveforms did not exceed the maximum allowed values and did not oscillate during turn on and turn off phases. The Gate-to-Source voltage also stayed within ± 300 mV of 12 V. during the on-resistance changes mentioned in Table 6.4. Due to events described in Chapter 6.3 the output of p-channel MOSFET control circuit responsible for transistor U6 was damaged.

6.3 Challenges and Modifications

Supply voltage for p-channel MOSFET gate control operational amplifiers was designed to be 20 V. The voltage was designed provided using programmable linear voltage regulator LM317T shown output of which could be configured by external resistor divider as shown in Figure 6.14 [64]. In the basic adjustable regulator configuration, the datasheet provides the following equation in order to program the output voltage [64]:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2, \tag{27}$$

where V_{OUT} is the output voltage, V_{REF} is the reference voltage 1.25 V, R_1 and R_1 are the external resistor dividers, and I_{ADJ} is the adjustment current.

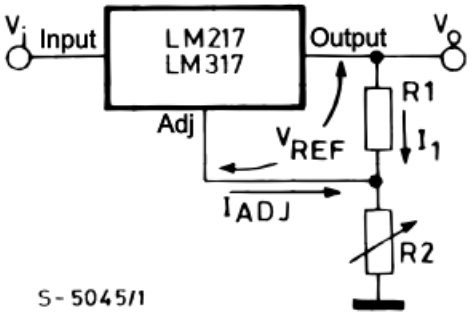


Figure 6.14: LM317 Basic adjustable regulator [64]

Due to I_{ADJ} being small by design, it can be ignored [64]. In order to provide 20 V, R_1 was chosen to be 240 Ω and R_2 was chosen to be a series connection of 360 Ω and 3.3 kΩ. Measured voltage with the selected resistors was measured to be 21.9 V however. The 360 Ω and 3.3 kΩ series connection was changed to series connection of 270 Ω and 2.7 kΩ. The new configuration yielded 19V, which was judged adequate as a supply voltage for the operational amplifiers in this test.

During the component creation in PADS the leads of KA7909TU were defined in wrong order. The mistake was solved by mounting the regulator sideways compared to the initial design. This error needs to be fixed if the MOSFET gate control board is to be redesigned.

Voltage follower operational amplifiers were designed to have a supply voltage of 28 V. The possibility of oscillation for these circuits was not accounted for in the design, which caused the voltage follower operational amplifiers to destroy the p-channel MOSFET control circuits due to the operational amplifiers in p-channel control circuits only having 19 V as the supply voltage. The supply voltage of the voltage followers was changed to 19 V after the p-channel MOSFET control operational amplifier was replaced. The initial designs of the circuits acting as voltage followers and control circuits for p-channel MOSFETs are illustrated in Figure 6.15 and Figure 6.16.

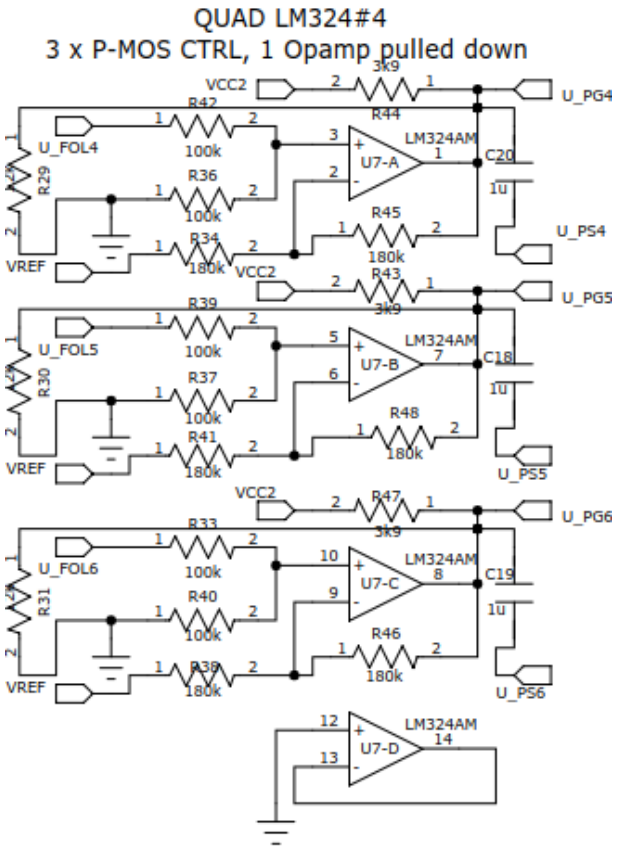


Figure 6.15 P-channel MOSFET control circuit

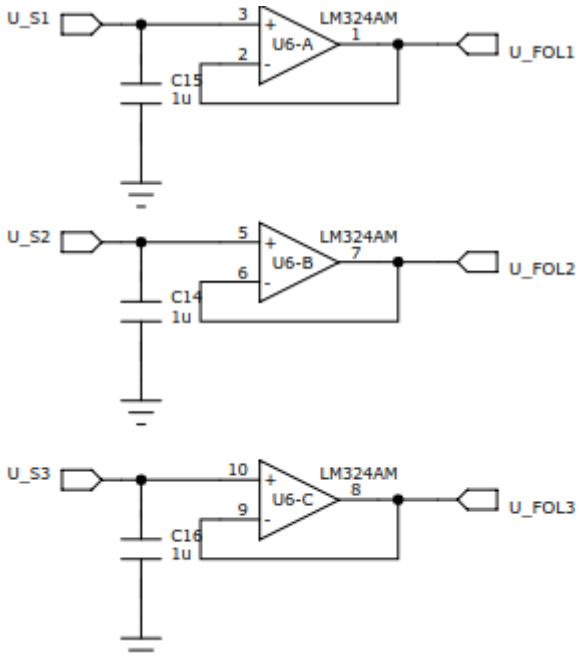


Figure 6.16 Voltage followers for n-channel MOSFETs

Capacitors chosen for the p-channel MOSFET control circuit in Figure 6.15 and the voltage follower input filter capacitors in Figure 6.16 initially caused ringing and caused the gate control voltage output for U6 to be internally shorted to negative supply rail in the LM324 responsible for p-channel MOSFET gate control voltages. The operational amplifier was replaced the second time. The capacitors were removed from the p-channel MOSFET control circuits and the voltage followers. After the removal of the capacitors the MOSFET control circuits had significant oscillations during the turn on and turn off events of the transistors. The turn-on and turn-off waveforms of the control circuits without the capacitors can be found in APPENDIX J. Adding a 20 µF ceramic capacitor to the non-inverting inputs of the voltage followers for the n-channel MOSFETs reduced the oscillations significantly.

Unknown, possibly supply voltage or voltage follower circuit related, event caused p-channel MOSFET control circuit to latch up and become unresponsive to input voltages, only producing high output. Operational amplifier was replaced the third time and 20V Zener diode was added between 20 V supply and 0 V. Additionally protection diodes were added from voltage follower outputs to 20 V supply before the p-channel MOSFET control circuit.

A single strand in the D-sub miniature connector wire became loose and punctured the heat shrink insulation shorting output U_PG6 to the drain of transistor U4. Presumably the short had caused the output swing of amplifier responsible for driving the gate of transistor U6 to be reduced significantly compared to the other outputs of the same amplifier. Due to the amplifier being changed three times prior, the pads on the PCB deteriorated significantly and judgement was made not to replace the amplifier due to it being able to fully open and close the transistor U6 even with the reduced output swing. The electrical characteristic of the designed system after the modifications are defined in Table 6.13.

Table 6.13 Electrical characteristics of the designed miniature test system

Parameter	Limit
MOSFET Gate Control Board +30V input,	Maximum 37 V Minimum 30 V
MOSFET Gate Control Board +20V input,	Maximum 37 V Minimum 22 V
MOSFET Gate Control Board -10V input,	Maximum -10 V Minimum -35 V
MOSFET Gate Control Board VREF output	Minimum 700 mV Maximum 14.7 V
MOSFET Gate Control U_G1, U_G2, U_G3 outputs	Minimum 700 mV Maximum 25.2 V
MOSFET Gate Control U_PG4, U_PG5 outputs	Minimum -8.1 V Maximum 16.4 V
MOSFET Gate Control U_PG6 (damaged) output	Minimum 1.5 V Maximum 13.4 V
MOSFET Gate Control U_S1, U_S2, U_S3, U_PS4, U_PS5, U_PS6 inputs	Minimum 0 V Maximum 18 V
Breakout Box	Maximum 30V (limited by the lugged 20-pin connectors [65])

A mistake in the design and wiring of Zener protection circuit in n-channel MOSFET gate voltage was noticed after the tests were concluded. Designed n-channel MOSFET gate control circuit is in Figure 6.17.

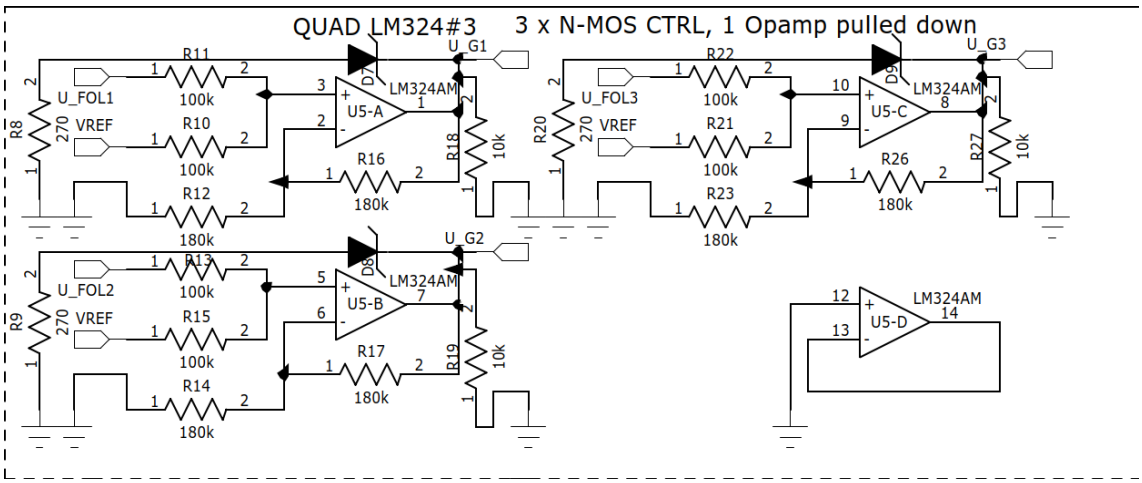


Figure 6.17 N-channel MOSFET gate control circuit.

Comparing Figure 5.10 and Figure 6.17 the lack of anode connection of the protection Zener diode can be noticed in the in the designed schematic. The connection was fixed with jumper wires after the tests described in this chapter were concluded. After the applied fix current consumption of the MOSFET Gate Control Board rose from 130 mA to over 220 mA. The maximum output of n-channel MOSFET Gate-to-Source voltages exceeded 17 V which is over the safe limit defined previously. After lowering the front resistor for potentiometer from 47 kΩ to 22 kΩ and connecting the front resistor and potentiometer series connection to 19 V instead of 28 V the maximum Gate-to-Source voltage was reduced to 12 V. However current consumption remained over 220 mA. Based on the current consumption the designed circuit protection had better performance than the one planned in PSpice.

Based on the tests, each of the designed n-channel MOSFET and p-channel MOSFET control voltage circuit needs to be tested for oscillations and maximum and minimum values. The measurement systems need to be redesigned. Unused operational amplifiers in the full-scale system version need to be pulled down in similar manner to the miniature test system due by connecting the non-inverting input to the ground potential and shorting the output to the inverting input. In the full-scale system the inputs and outputs were simply designed to be grounded. Off-state current measurement resistors need to be moved to the low side compared to the components in test in order to improve the measurement resolution.

6.4 Summary

A semiconductor measurement system was designed and built mostly successfully. Due to the mistakes in design and implementation, the mounting style parts of the system needed to be changed based on the tests if the system is redesigned. In particular the supply voltages of the operational amplifiers in voltage follower configuration in front of p-channel MOSFET gate control circuits need to be lowered to the same voltage as the p-channel MOSFET driving operational amplifiers or lower.

Most of the component parameters measured while the component was defined to be in conducting state were within the values specified in the datasheets. Exclusions were on-resistance of the uppermost n-channel MOSFET transistor in the series connection and two threshold voltage measurements of the n-channel MOSFET transistors.

Due to the leakage current resistors being on the high side in comparison to the devices under test, the leakage current resistors lacked precision. The system needs to be redesigned so that the leakage current resistors are placed on the low side.

Instead of MOSFET gate driving circuit being rather universal based on the simulations of the full-scale system, in which the same gate voltage control circuits were used for each of the series connections, the individual gate voltage driving circuits or voltage followers may oscillate damaging the components on the MOSFET gate control board and possibly even the components on the measurement board. After the addition of input filters the MOSFET gate control card fit the required parameters in particular the minimum and maximum output voltage requirements defined for the full-scale system in Table 5.30. A mistake was made in the protection Zener diode wiring which needs to be corrected if the system was to be redesigned. The MOSFET gate control board needs to be thoroughly tested if the full-scale test system is redesigned.

7 CONCLUSIONS

In this thesis, the passivation methods mainly researched by RUAG Space Finland and European Space Agency were introduced and explained. Passivation can be performed on different levels of the spacecraft mainly by disconnecting, discharging or shorting the power storages on board of the satellite. The passivation function can be performed using relays, MOSFETs, bypass switches or cable cutters. Diodes may also be used in conjunction with other passivation methods in order to rectify the currents. Each of the switch component types has advantages and disadvantages which need to be considered in the design of passivation function implementation.

Due to long life-time data being unavailable in cases of semiconductors and relays during the writing of this thesis artificial temperature aging tests were proposed. In addition to artificial aging tests switching voltage tests on bypass switches and extended temperature range tests in the case of relays were proposed to be performed.

The durations of tests calculated based on the defined field conditions and formulae that were defined to be applicable in the worst possible cases of the field conditions. The total duration of tests was calculated to be over 8 months and in combination with long lead times of space grade components the tests and designs could not be finished by the end of the writing process of this thesis.

The semiconductor portion of the test system was designed independently based on the test plan drafts created during the MSc thesis work done for RUAG Space Finland. The test system was mainly designed to consist of a heat resistant measurement board for the components in the tests placed in the thermal chamber, a breakout box from which the measurement board would be interfaced in regards to measurements and control voltages and MOSFET gate control board. The gate control board would keep the Gate-to-Source voltages of the transistors constant during the phase where the MOSFETs would be defined to be in open-state.

A miniature version of the proposed semiconductor test setup was designed and built by using the funding of Electronics and Communications Department of Tampere University of Technology. The constructed system provided useful info which could be used to redesign parts of the system to improve measurement resolution and remove flaws in the design which would have had the potential to damage the full-scale system if the system was built. The measurements performed using the system were within the specified datasheet limits for the most of the cases.

In order to improve the performance of the designed test system several changes should be made. Breakout box leakage current measurement resistors need to be placed on low side compared to the devices under tests to enable the selection of more accurate measurement channel for the oscilloscopes compared to one used in the test. KA7909TU model needs to be corrected for correct mounting. Feedback resistors of the LM317 designed to provide 20 V need to be changed to values defined in chapter 6.3. Feedback capacitors of the p-channel MOSFET voltage control circuit need to be removed. Capacitors on the non-inverting inputs of the operational amplifiers used as voltage followers in n-channel MOSFET gate control circuits need to be changed to 20 µf. Zener protection circuits need to be redesigned. Heat sink mounting needs to be equalized across the components based on the case temperature differences in nominal mission phase particularly in the case of MOSFETs. Possible future tasks to be done on the measurement setup in addition to redesigning the parts of the breakout box and the MOSFET gate control board would be incorporating a thermal equalizing system for the semiconductors in the life test.

REFERENCES

[1] International Standardization Organization, Space Systems, Space Debris Mitigation Requirements, ISO 24113, Standard, Second Edition, 15.05.2011, Access Restricted, preview [WWW] https://www.iso.org/obp/ui/#iso:std:iso:24113:ed-2:v1:en, reference date 15.11.2017

[2] Space Debris by Numbers, ESA's Space Debris Office at ESOC, Darmstadt, Germany [WWW] http://www.esa.int/Our_Activities/Operations/Space_Debris/Space_debris_by_the_numbers, reference date 5.9.2017

[3] United Nations Office of Space Affairs, Space Debris Mitigation Standards Adopted by States and International Organizations, Compendium, 6.4.2017, [WWW] http://www.unoosa.org/documents/pdf/spacelaw/sd/Space_Debris_Compendium_COPUOS_6_-April-2017.pdf, reference date 15.11.2017

[4] European Committee for Space Standardization, Adoption Notice of ISO 24113: Space systems - Space debris mitigation requirements, ECSS-U-AS-10C, Standard, 10.02.2012, Access Restricted

[5] ESA Director General's Office, Space Debris Mitigation Policy for Agency Projects, Policy, ESA/ADMIN/IPOL(2014)2, 28.3.2014, Paris, France, [WWW] http://www.iadc-online.org/References/Docu/admin-ipol-2014-002e.pdf, reference date 22.11.2017

[6] ESA Space Debris Office, ESA's Annual Space Environment Report, Technical Note, 27.4.2017, European Space Operations Centre,Robert-Bosch-Strasse 5, D-64293 Darmstadt, Germany, [WWW] https://www.sdo.esoc.esa.int/environment_report/Environment_Report_I1R2_20170427.pdf, reference date 4.9.2017

[7] ESA Space Debris Mitigation WG, ESA Space Debris Mitigation Compliance Verification Guidelines, Handbook, 19.2.2015, ESTEC, European Space Research and Technology Centre Noordwijk, The Nedtherlands [WWW] http://www.iadc-online.org/References/Docu/ESSB-HB-U-002-Issue1(19February2015).pdf, reference date 30.6.2017

[8] Emilio Lapeña, Daniel Ruf, José Luis Herranz, Fernando Gómez-Carpintero, Miguel Rodríguez, José Otero, Passivation Strategies, on board Airbus DS LEO PCDUs, Conference Proceedings, 11th European Space Power Conference, 3-7.10.2016, Thessaloniki, Greece E3S Web of Conferences 16, 13003 (2017), 23.5.2017, [WWW] https://www.e3s-conferences.org/articles/e3sconf/pdf/2017/04/e3sconf_espc2017_13003.pdf, reference date 15.11.2017

[9] François Bausier, Ferdinando Tonicello, Tiago Soares, Passivation of Spacecraft Electrical Power System at End of Mission, Conference Proceedings, 10th European Space Power Conference, 13.-17.8.2014, Noordwijkerhout, Netherlands. Edited by L. Ouwehand, ESA-ESTEC, [WWW] http://articles.adsabs.harvard.edu/full/2014ESASP.719E..67B, reference date 30.6.2017

[10] François Bausier, Passivation of spacecraft power system at end of mission, Technical Note, 18.7.2013, European Space Agency, European Space Research and Technology Centre, Noordwijk, The Netherlands, Access Restricted, reference date 30.6.2017

[11] Michelle A. Manzo, Jeffrey C. Brewe, Ratnakumar V. Bugga, Eric C. Darcy and Judith A. Jeevarajan, Barbara I. McKissock, Paul C. Schmitz, NASA Aerospace Flight Battery Program, Generic Safety, Handling and Qualification Guidelines for Lithium-Ion (Li-Ion) Batteries Availability of Source Materials for Lithium-Ion (Li-Ion) Batteries Maintaining Technical Communications Related to Aerospace Batteries (NASA Aerospace Battery Workshop),Technical Report,10.7.2008, NASA Engineering and Safety Center Technical Report, Glenn Research Center, Cleveland, Ohio, Marshall Space Flight Center, Huntsville, Alabama, Jet Propulsion Laboratory, Pasadena, California Johnson Space Center, Houston, Texas, NASA/TM-2010-216727/Volume II, [WWW] https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20100028067.pdf, reference date 16.11.2017

[12] Simola Juhani, Spacecraft Power System Passivation, D6 Preliminary assessment of battery safety, Technical Note, 19.9.2015, RUAG Space Finland, Access Restricted

[13] Joe Troutman, ABSL Performance Comparison SONY 18650 Hard Carbon Cell and SONY 18650 Hard Carbon Mandrel Cell, Presentation, ABSL Space Products 2011, NASA Aerospace Battery Workshop, 2011, [WWW] https://batteryworkshop.msfc.nasa.gov/presentations/01_ABSL%202011%20NASA%20Battery%20Workshop.pdf, reference date 16.11.2017

[14] E. Mosset, Active and Autonomous Balancing System for Satellites Batteries, Saft, Space and Defence Division, Proceedings of the 9th European Space Power Conference, 6-10.6.2010 Saint Raphael, France, [WWW] http://articles.adsabs.harvard.edu/full/2011ESASP.690E.100M, reference date 16.11.2017

[15] Emmanuel Bonneau, Stéphane Remy, SAFT VES16 Solution for Small GEO, Conference Proceedings, 11th European Space Power Conference, 3-7.10.2016, Thessaloniki, Greece 3-7.10.2016 Saft, Space and Defence Division, E3S Web of Conferences 16, 06004 (2017), [WWW] https://www.e3s-conferences.org/articles/e3sconf/pdf/2017/04/e3sconf_espc2017_06004.pdf, reference date 16.11.2017

[16] Douay, N., Galileo IOV Electrical Power Subsystem Relies On Li-Ion Battery Charge Management Controlled By Hardware, Conference Proceedings, 9th European Space Power Conference, 6-10.6.2011, Saint Raphael, France, ESA SP, Vol. 690, [WWW] http://articles.adsabs.harvard.edu/full/2011ESASP.690E.144D, reference date 16.11.2017

[17] François Bausier, Maria Nestoridi, Bruno Samaniego, Juhani Simola, Andrew Wolahan, Spacecraft Electrical Passivation: From Study to Reality, Conference Proceedings, 23.5.2017, E3S Web Conf. Volume 16, 2017 11th European Space Power Conference, ESA-ESTEC, Airbus Defense and Space, RUAG Space Finland, [WWW] https://www.e3s-conferences.org/articles/e3sconf/pdf/2017/04/e3sconf_espc2017_13002.pdf, reference date 30.6.2017

[18] Airbus DS Thermal Section, Stéphane Iugovich, Jean-Baptiste Bernaudin, Bruno Samaniego Lopez, D3 Assessment of S/C temperature after passivation, Technical Note, created 15.06.2015, approved 22.6.2015, Airbus DS, Access Restricted

[19] François Bausier, Highlights on Electrical Passivation, Workshop Estec, EoL Electrical Passivation, 11.10.2013, Access Restricted

[20] Myllymäki Harri, Simola Juhani, Karinsalo Ritva, Kuitunen Juha, D7 Review of Potential Implementations & Selection, Technical Note, created 3.9.2015, approved 4.9.2015, RUAG Space Finland, Access Restricted

[21] Myllymäki Harri, Simola Juhani, Karinsalo Ritva, Kuitunen Juha, D5 Long Term Behaviour of Components and Test Plan, Technical Note, created 3.9.2015, approved 4.9.2015, RUAG Space Finland, Access Restricted

[22] United States of America Department of Defense, Military Handbook Electronic Reliability Design Handbook, Handbook, 1.10.1998, United States of America Department of Defense, [WWW] http://www.sre.org/pubs/Mil-Hdbk-338B.pdf, reference date 25.6.2017

[23] B. Todd, S. Uznanski, Radiation Risks and Mitigation in Electronic Systems, Published by CERN in the Proceedings of the CAS-CERN Accelerator School: Power Converters, Baden, Switzerland, 7.5.2014–14.5.2014, edited by R. Bailey, CERN-2015-003 (CERN, Geneva, 2015), [WWW] https://cds.cern.ch/record/2038628/files/245-263-Todd.pdf, reference date 20.10.2018

[24] ECSS Secretariat ESA-ESTEC Requirements & Standards Division, ECSS-E-ST-10-12C, Space engineering Methods for the calculation of radiation received and its effects, and a policy for design margins, 15.11.2008, Standard, European Cooperation for Space Standardization, Noordwik, The Netherlands, [WWW] https://www.abbottaerospace.com/wpdm-package/ecss-e-st-10-12c-space-engineering-methods-for-the-calculation-of-radiation-received-and-its-effects-and-a-policy-for-design-margins?wpdmdl=41647&ind=1508511692345, reference date 20.10.2018

[25] ECSS Secretariat ESA-ESTEC Requirements & Standards Division, ECSS-E-HB-10-12A, Space engineering Methods for the calculation of radiation received and its effects, and a policy for design margins, Handbook, 17.12.2010, [WWW] https://www.abbottaerospace.com/wpdm-package/ecss-e-hb-10-12a-space-engineering-calculation-of-radiation-and-its-effects-and-margin-policy-handbook?wpdmdl=41596&ind=1508442355687, reference date 20.10.2018

[26] D. J. Cochran et al., "Total Ionizing Dose and Displacement Damage Compendium of Candidate Spacecraft Electronics for NASA," 2009 IEEE Radiation Effects Data Workshop, Quebec City, QC, 2009, pp. 25-31.doi: 10.1109/REDW.2009.5336318, [WWW] https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20110015251.pdf, reference date: 20.10.2018

[27] Megan C. Casey1, Jean-Marie Lauenstein1, Robert A. Gigliuto2, Edward P. Wilcox2, Anthony M. Phan2, Hak Kim2, Dakai Chen1, and Kenneth A. LaBel1, Destructive Single-Event Failures in Schottky Diodes, NEPP Electronic

Technology Workshop 17-19.6.2014, Greenbelt, MD, [WWW] https://nepp.nasa.gov/files/26196/2014-561-Casey-Final-Web-Pres-ETW-Diodes-TN16278_v2.pdf, reference date 20.10.2018

[28] ECSS Secretariat ESA-ESTEC Requirements & Standards Division, ECSS-Q-ST-30-02C, Space product assurance Failure modes, effects (and critically) analysis (FMEA/FMECA), Standard, 6.3.2009, European Cooperation for Space Standardization, Noordwik, The Netherlands, [WWW] http://www.ecss.nl/wp-content/uploads/standards/ecss-q/ECSS-Q-ST-30-02C6March2009.pdf, reference date 28.6.2017.

[29] Norris, K C, and AH Landzberg. "Reliability of Controlled Collapse Interconnections." IBM Journal of Research and Development 13, no. 3 (1969): 266-271

[30] JEDEC, Arrhenius equation (for reliability), Definition [WWW] https://www.jedec.org/standards-documents/dictionary/terms/arrhenius-equation-reliability, reference date 20.10.2018

[31] Esterline, M402, RELAY LATCH 4 PDT/ 10 AMP(15* AMP), Datasheet, [WWW] http://eu.leachint.fr/wp-content/uploads/2015/03/hermetically-sealed-relay-relais-hermetique-M402.pdf, reference date 6.9.2017

[32] DRI, EL210/EL215 Series, 2PDT, 10/15 AMP, pp. 8-13, Datasheet, [WWW] https://first-switchtech.com/datasheets/EL215.pdf, reference date 6.9.2017

[33] Esterline, GP250, RELAY LATCH, 2 PDT/ 2 AMP-50V, Datasheet, [WWW] http://www.flamecorp.com/PDF/Esterline-Leach/Leach,GP250.pdf , reference date 6.9.2017

[34] REL, Series TL, Ultraminiature «TO 5 transistor size» magnetic latching relays 28 V / 1 A, Datasheet, [WWW] https://first-switchtech.com/datasheets/TL.pdf, reference date 6.9.2017

[35] ST, STRH100N10, Rad-Hard 100V, 48 A N-channel Power MOSFET, Datasheet, [WWW] http://www.st.com/content/ccc/resource/technical/document/datasheet/ef/6c/4b/d8/30/50/43/58/CD00273200.pdf/files/CD00273200.pdf/jcr:content/translations/en.CD00273200.pdf, reference date 6.9.2017

[36] ST, STRH40P10, Rad-Hard P-channel 100V, 34 A Power MOSFET, Datasheet, [WWW]

http://www.st.com/content/ccc/resource/technical/document/datasheet/0a/e5/8a/96/8c/47/41/70/CD00295131.pdf/files/CD00295131.pdf/jcr:content/translations/en.CD00295131.pdf, reference date 6.9.2017

[37] International Rectifier, IRHMS57160 JANSR2N7471T1 100V, N-CHANNEL, RADIATION HARDENED POWER MOSFET THRU-HOLE (Low-Ohmic TO-254AA), Datasheet, [WWW] http://www.irf.com/product-info/datasheets/data/irhms57160.pdf, reference date 6.9.2017

[38] International Rectifier, IRHMS67260 JANSR2N7584T1 200V, N-CHANNEL, RADIATION HARDENED POWER MOSFET THRU HOLE (Low-Ohmic TO-254AA), Datasheet, [WWW] http://www.irf.com/product-info/datasheets/data/irhms67260.pdf, reference date 6.9.2017

[39] International Rectifier, IRHMS57064 JANSR2N7470T1 60V, N-CHANNEL RADIATION HARDENED POWER MOSFET THRU-HOLE (Low-Ohmic TO-254AA), Datasheet, [WWW] http://www.irf.com/product-info/datasheets/data/irhms57064.pdf, reference date 13.11.2017

[40] International Rectifier, IRFM9140 JANTX2N7236 JANTXV2N7236 JANS2N7236100V, P-CHANNEL POWER MOSFET THRU-HOLE (TO-254AA), Datasheet, [WWW] http://www.irf.com/product-info/datasheets/data/irfm9140.pdf, reference date 13.11.2017

[41] Vishay, SQJ402EP Automotive N-Channel 100 V (D-S) 175 °C MOSFET, Datasheet, [WWW] https://www.vishay.com/docs/67997/sqj402ep.pdf, reference date 13.10.2018

[42] ON Semiconductor, FDB3652-F085 N-Channel PowerTrench® MOSFET 100V, 61A, 16mΩ, Datasheet, [WWW] http://www.onsemi.com/pub/Collateral/FDB3652_F085-D.PDF, reference date 13.10.2018

[43] ST, SCTW100N65G2AG Automotive silicon carbide Power MOSFET 650 V, 100 A, 22 mΩ (typ., TJ=150 °C), in an HiP247™ package, Datasheet-preliminary data, [WWW] https://www.st.com/resource/en/datasheet/sctw100n65g2ag.pdf, reference date 13.10.2018

[44] ST, STPS20100HR, Aerospace 1 x 20 and 2 x 20 A - 100 V Schottky rectifier, Datasheet, [WWW] http://www.st.com/content/ccc/resource/technical/document/datasheet/66/1c/a9/

6a/87/4b/49/a8/CD00260945.pdf/files/CD00260945.pdf/jcr:content/translations/en.CD00260945.pdf, reference date 6.9.2017

[45] International Rectifier, 45CKQ100 45A*, 100V,SCHOTTKY RECTIFIER HIGH EFFICIENCY SERIES, Datasheet, [WWW] http://www.irf.com/product-info/datasheets/data/45ckq100.pdf, reference date 6.9.2017

[46] International Rectifier, 16CYQ100C JANS1N7070CCT3 JANTX1N7070CCT3 JANTXV1N7070CCT3, SCHOTTKY RECTIFIE HIGH EFFICIENCY SERIES 16Amp, 100V, Datasheet, [WWW] http://www.irf.com/product-info/datasheets/data/16cyq100c.pdf, reference date 13.11.2017

[47] ST, STPSC20H065C 650 V power Schottky silicon carbide diode, Datasheet,[WWW] https://www.st.com/resource/en/datasheet/stpsc20h065c.pdf, reference date 13.10.2018

[48] ECSS-Q-ST-30-11C, Space product assurance, Derating – EEE components, European Cooperation for Space Standardization, Standard, Rev 1, 4.10.2011, ECSS Secretariat ESA-ESTEC Requirements & Standards Division, Noordwijk, The Netherlands, [WWW] https://escies.org/download/webDocumentFile?id=58751, reference date 6.9.2017

[49] ECSS-Q-ST-70-12C, Space product assurance, Design rules for printed circuit boards, European Cooperation for Space Standardization, 14.7.2014, ECSS Secretariat ESA-ESTEC Requirements & Standards Division, Standard, Noordwijk, The Netherlands, [WWW] https://escies.org/download/webDocumentFile?id=62466, reference date 14.10.2018

[50] IPC, IPC-2152 — Standard for Determining Current-carrying Capacity in Printed Board Design Released, IPC — Association Connecting Electronics Industries®, BANNOCKBURN, Ill., USA, 24.9.2009, Web page, [WWW] https://www.ipc.org/ContentPage.aspx?pageid=IPC-2152-Standard-for-Determining-Current-carrying-Capacity-in-Printed-Board-Design-Released, reference date 14.10.2018

[51] Helukabel, SiHF silicon multicore cable, flexible, halogen-free, meter marking, Datasheet, [WWW] http://www.helukabel.com/opc/workarea/suppliers/STD/documents/pdf/db/1DB_22989_en.pdf, reference date 14.10.2018

[52] LappGroup, T12 Power ratings and conversion factors of cables and wires acc. VDE 0298-4, Techincal Table, Mdmetric http://mdmetric.com/elect/T12_Power_Rating_Basic_Table_Reduction_Tables.pdf, assumed to be from 2016-2017 catalog, reference date 14.10.2018

[53] VDE Verlag, DIN VDE 0298-4 VDE 0298-4:2003-08 Application of cables and cords in power installations Part 4: Recommended current-carrying capacity for sheathed and nonsheathed cables for fixed wirings in and around buildings and for flexible cables and cords, Withdrawn standard, Access Restricted, 8.2003, preview https://www.vde-verlag.de/standards/0298010/din-vde-0298-4-vde-0298-4-2003-08.html, reference date 14.10.2018

[54] LappGroup, T12_Current_ratings_basic_table_reduction_tables, Technical table, 2018, [WWW] https://t3.lappcdn.com/fileadmin/catalog/2018_int_pdf/T12_Current_ratings_basic_table_reduction_tables.pdf, reference date 14.10.2018

[55] VDE Verlag, DIN VDE 0298-4 VDE 0298-4:2013-06 Application of cables and cords in power installations. Part 4: Recommended current-carrying capacity for sheathed and nonsheathed cables for fixed wirings in and around buildings and for flexible cables and cords, Standard, Access Restricted, 6.2013, preview [WWW] https://www.vde-verlag.de/standards/0298016/din-vde-0298-4-vde-0298-4-2013-06.html, reference date 14.10.2018

[56] ITT Cannon, Datasheet for part number DCMM37PM, Datasheet, [WWW] https://media.digikey.com/pdf/Data%20Sheets/ITT%20PDFs/DCMM37PM.pdf , reference date: 15.10.2018

[57] Molex, FHTxx*1)S5Gy*2), Datasheet, [WWW] https://media.digikey.com/pdf/Data%20Sheets/Molex%20PDFs/FHTxxS5Gy.pdf, reference date 15.10.2018

[58] ON Semiconductor, LM324, LM324A, LM324E, LM224, LM2902, LM2902E, LM2902V, NCV2902, Datasheet, [WWW] https://www.onsemi.com/pub/Collateral/LM324-D.PDF, reference date 16.10.2018

[59] Farnell, LM324DR2G - Operational Amplifier, Quad, 4 Amplifier, 1 MHz, 0.6 V/µs, 3V to 32V, SOIC, 14 Pins, Store Page, [WWW] https://fi.farnell.com/on-semiconductor/lm324dr2g/op-amp-quad-1mhz-0-6v-us-14soic/dp/2295979, reference date 16.10.2018

[60] Vishay Siliconix, IRF610, SiHF610 Power MOSFET, Datasheet, [WWW] http://www.farnell.com/datasheets/2046306.pdf, reference date 17.10.2018

[61] Vishay Siliconix, IRF9630, SiHF9630 Power MOSFET, Datasheet, [WWW] http://www.farnell.com/datasheets/2364225.pdf, reference date 17.10.2018

[62] ST, FERD30M45C Field effect rectifier, Datasheet, [WWW] http://www.farnell.com/datasheets/2342756.pdf, reference date 17.10.2018

[63] Toshiba, Power MOSFET Thermal Design and Attachment of a Thermal Fin, Application Notes, [WWW] https://toshiba.semicon-storage.com/info/docget.jsp?did=13417, reference date 17.10.2018

[64] ST, LM217, LM317, 1.2 V to 37 V adjustable voltage regulators, Datasheet, [WWW] https://www.st.com/resource/en/datasheet/lm217.pdf, reference date 17.10.2018

[65] Multicomp, IDC Header Lugged 20 Way, Datasheet, [WWW] http://www.farnell.com/datasheets/1677351.pdf, reference date 18.10.2018

APPENDIX A: SEMICONDUCTOR MEASUREMENT BOARD

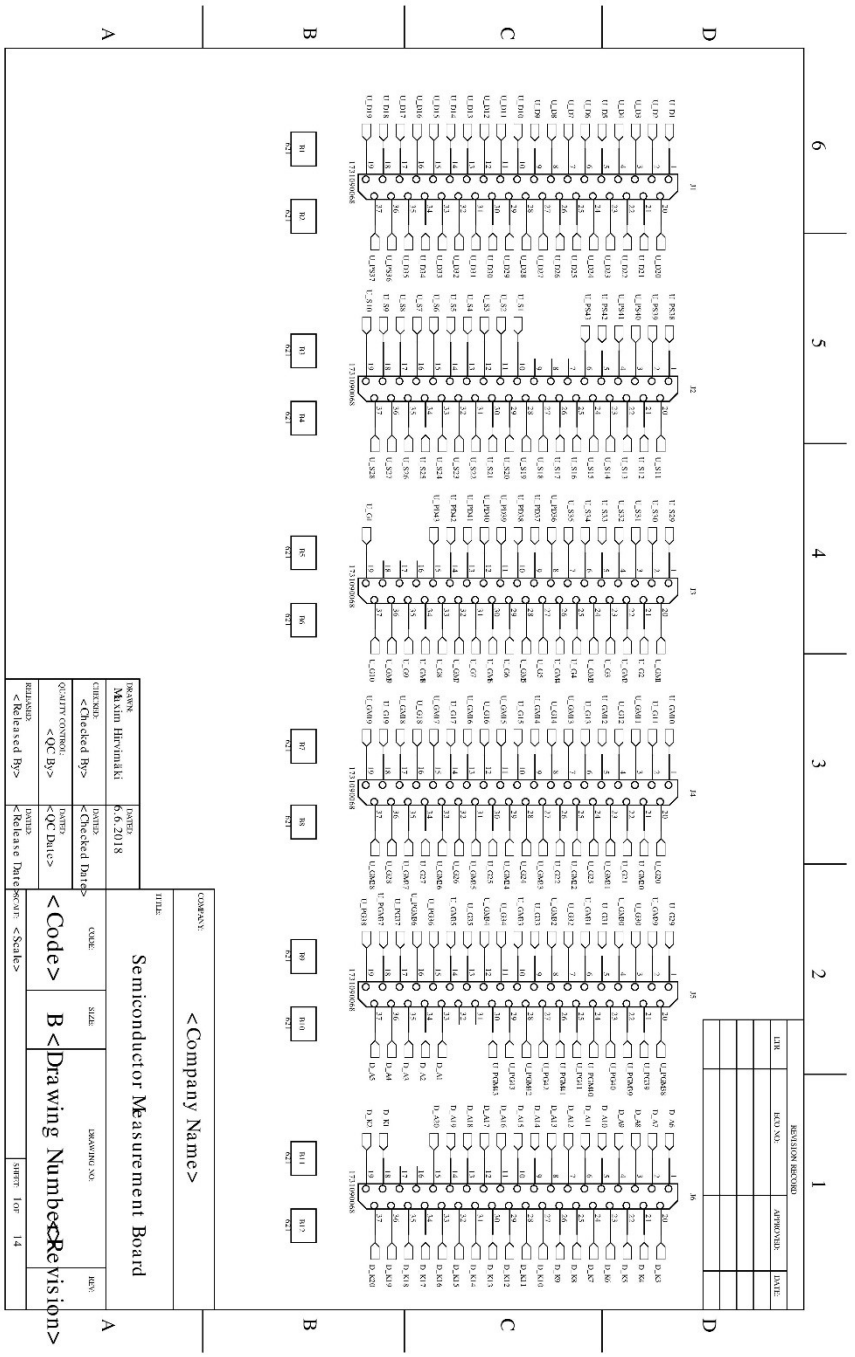


Figure A. 1 Semiconductor Measurement Board Schematic page 1

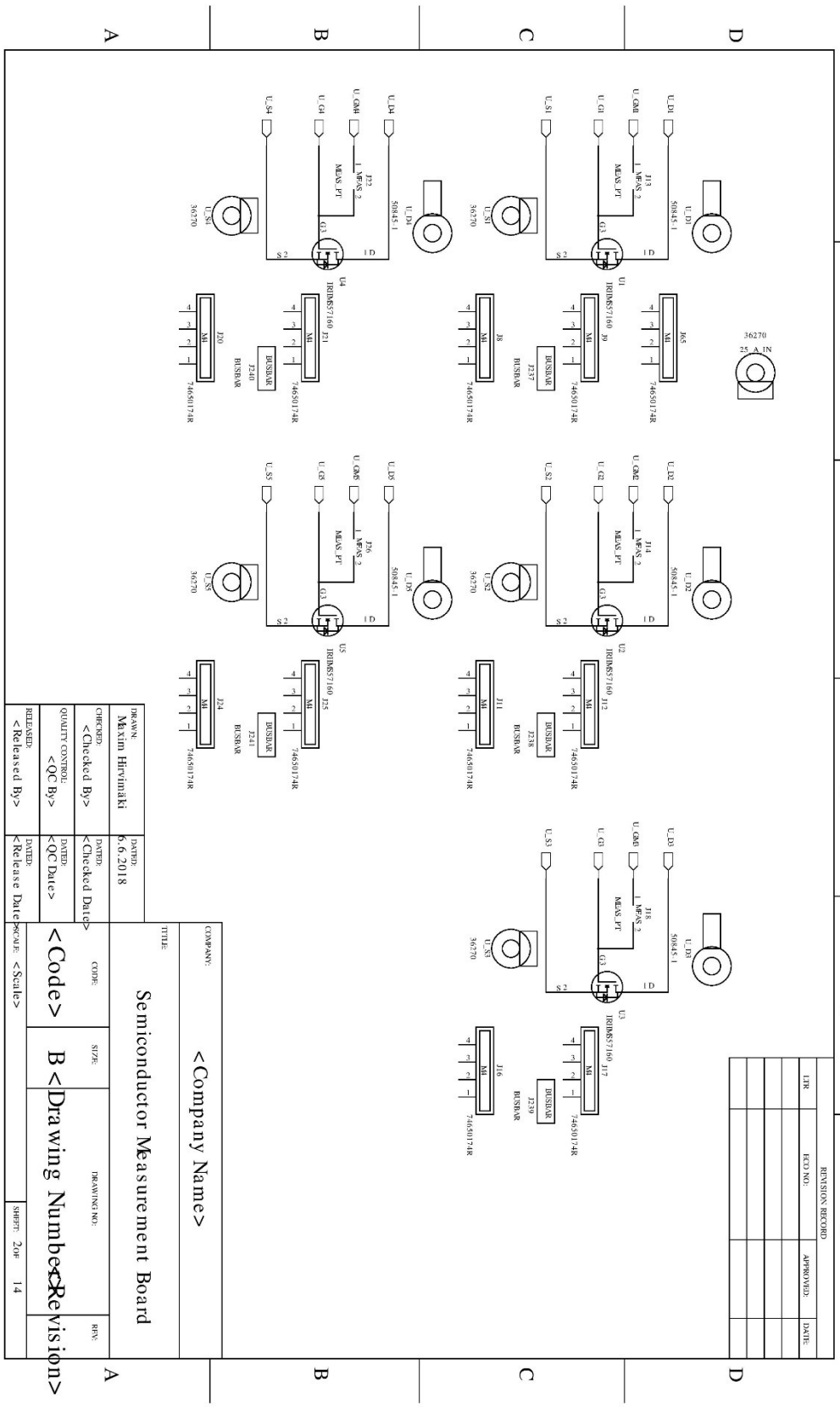


Figure A. 2 Semiconductor Measurement Board Schematic page 2

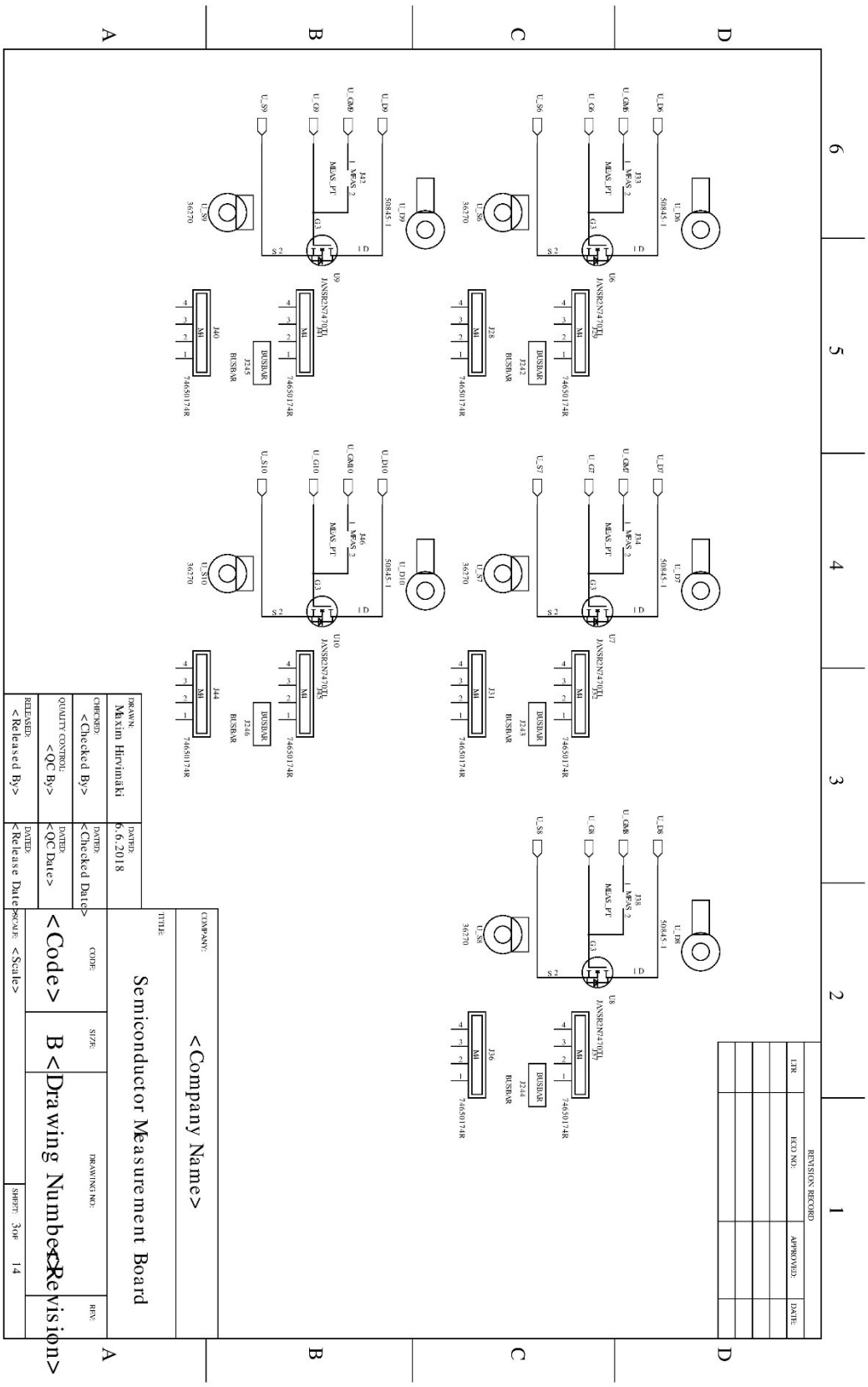


Figure A. 3 Semiconductor Measurement Board Schematic page 3

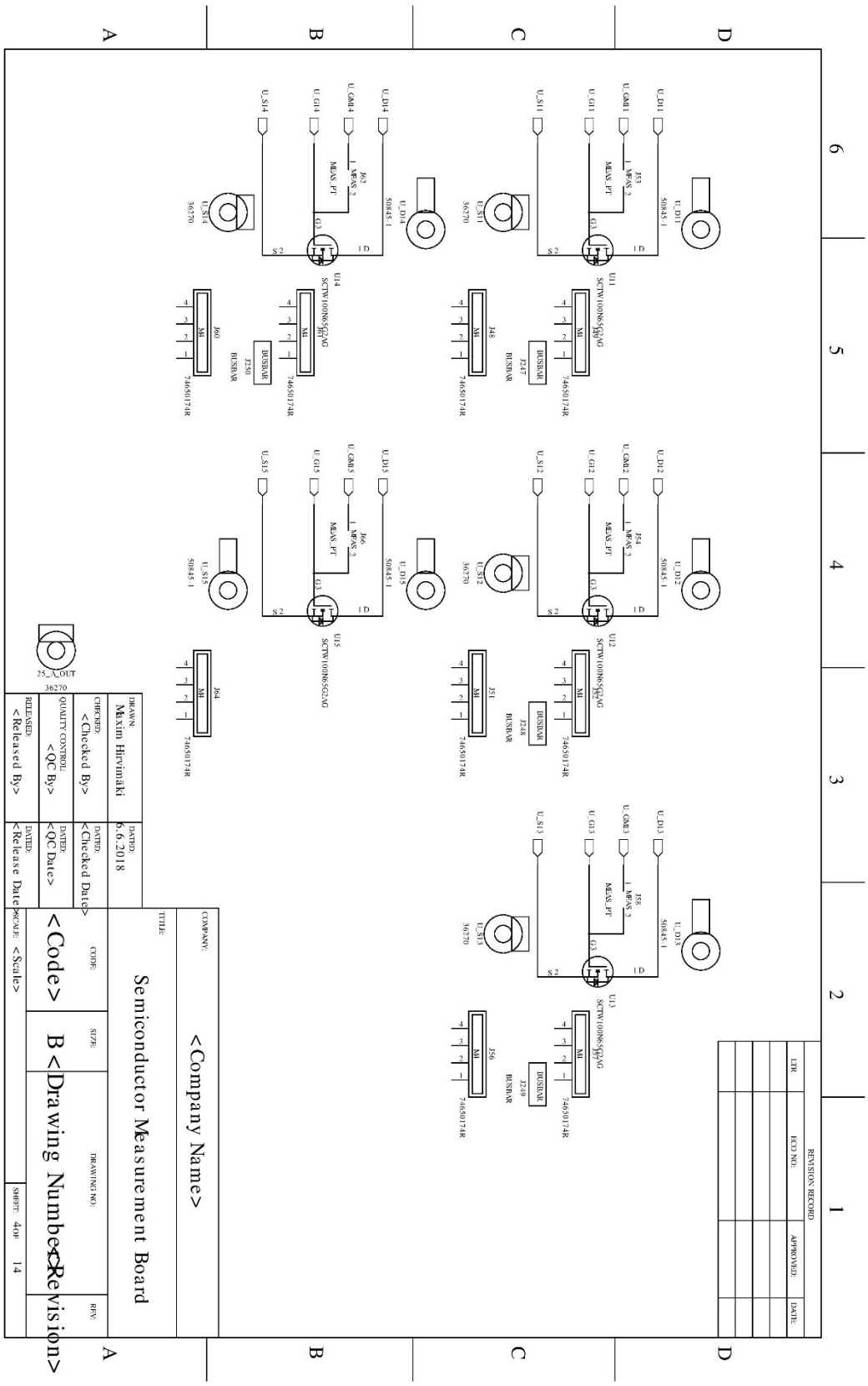


Figure A. 4 Semiconductor Measurement Board Schematic page 4

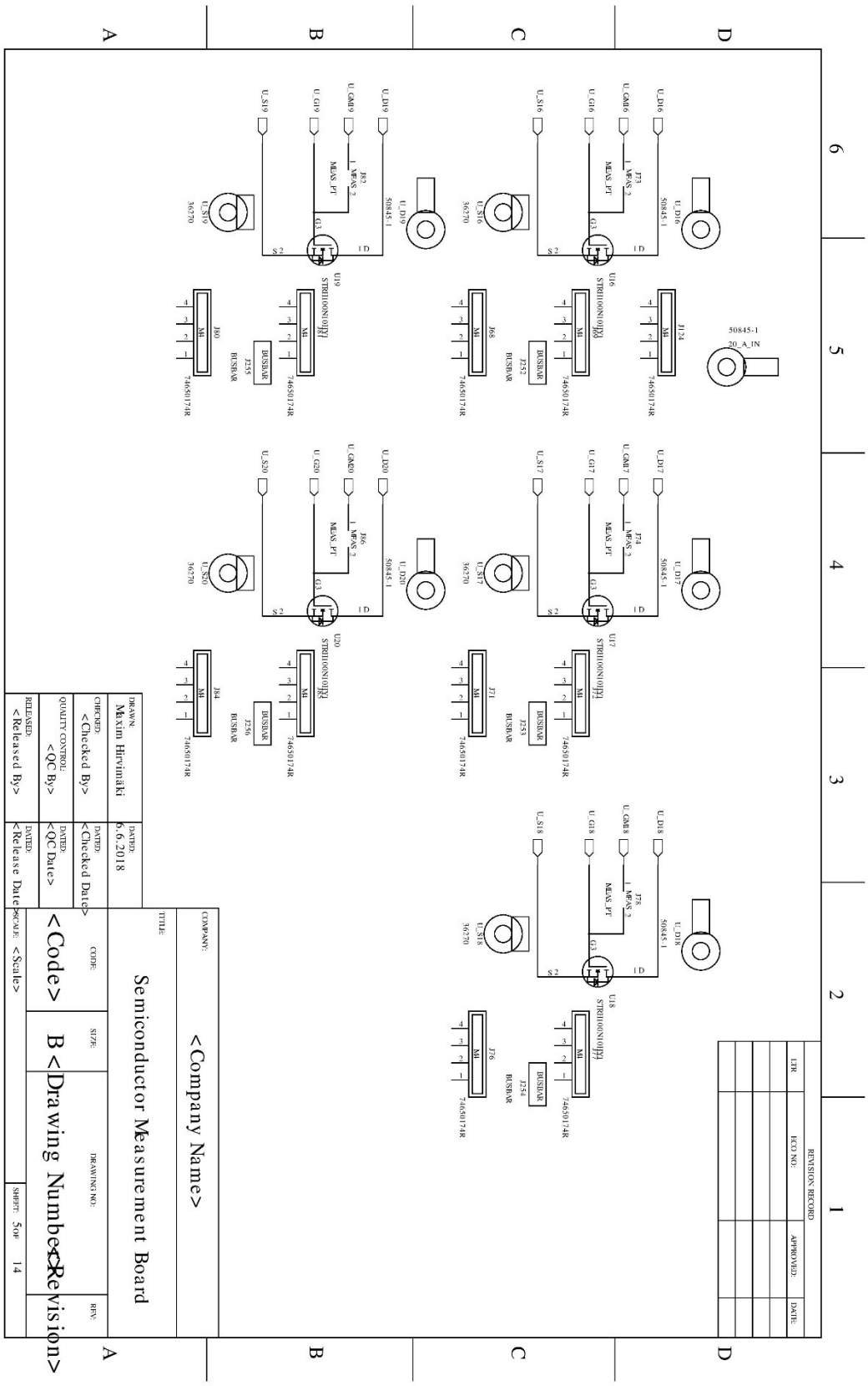


Figure A. 5 Semiconductor Measurement Board Schematic page 5

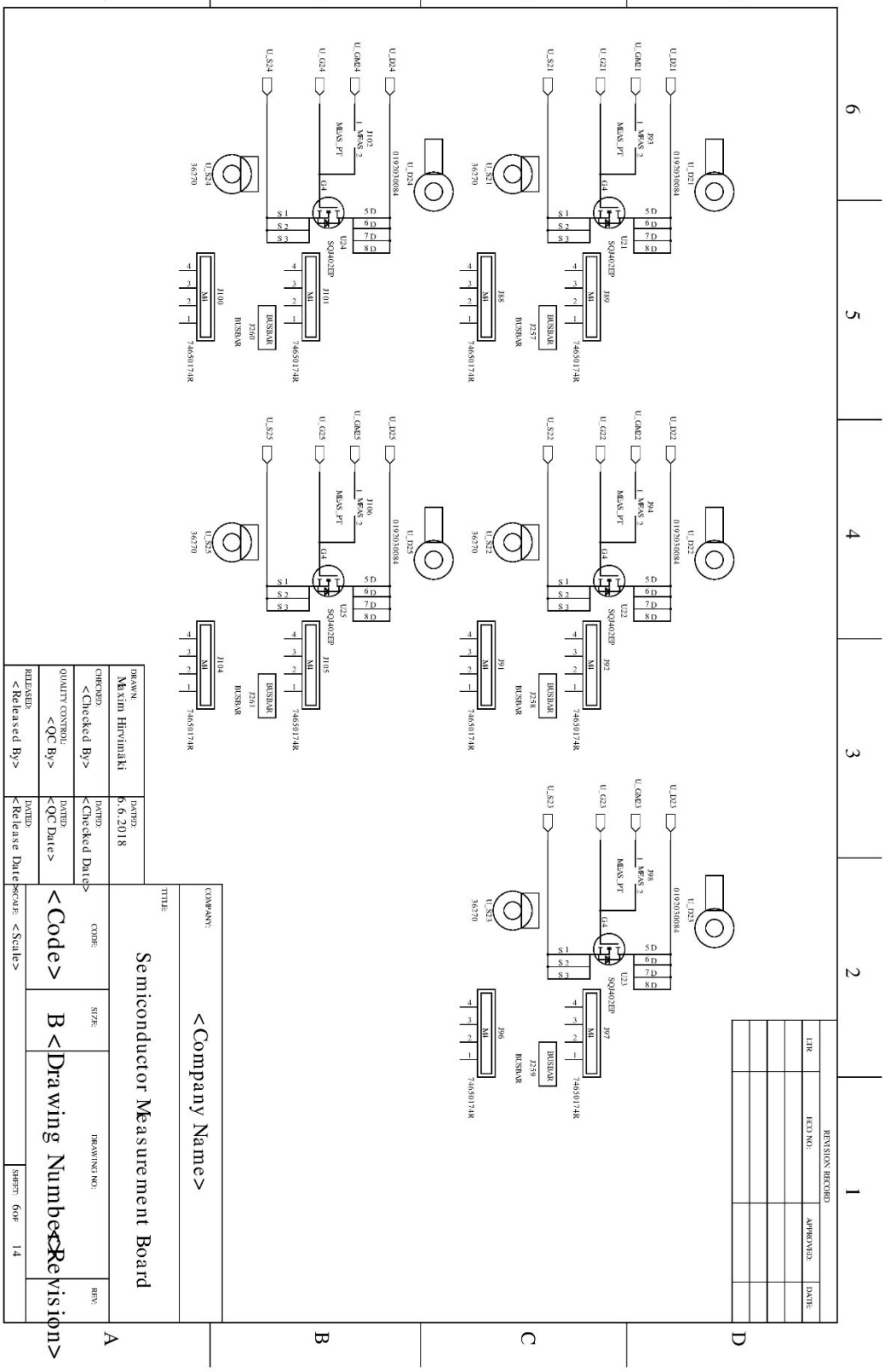


Figure A. 6 Semiconductor Measurement Board Schematic page 6

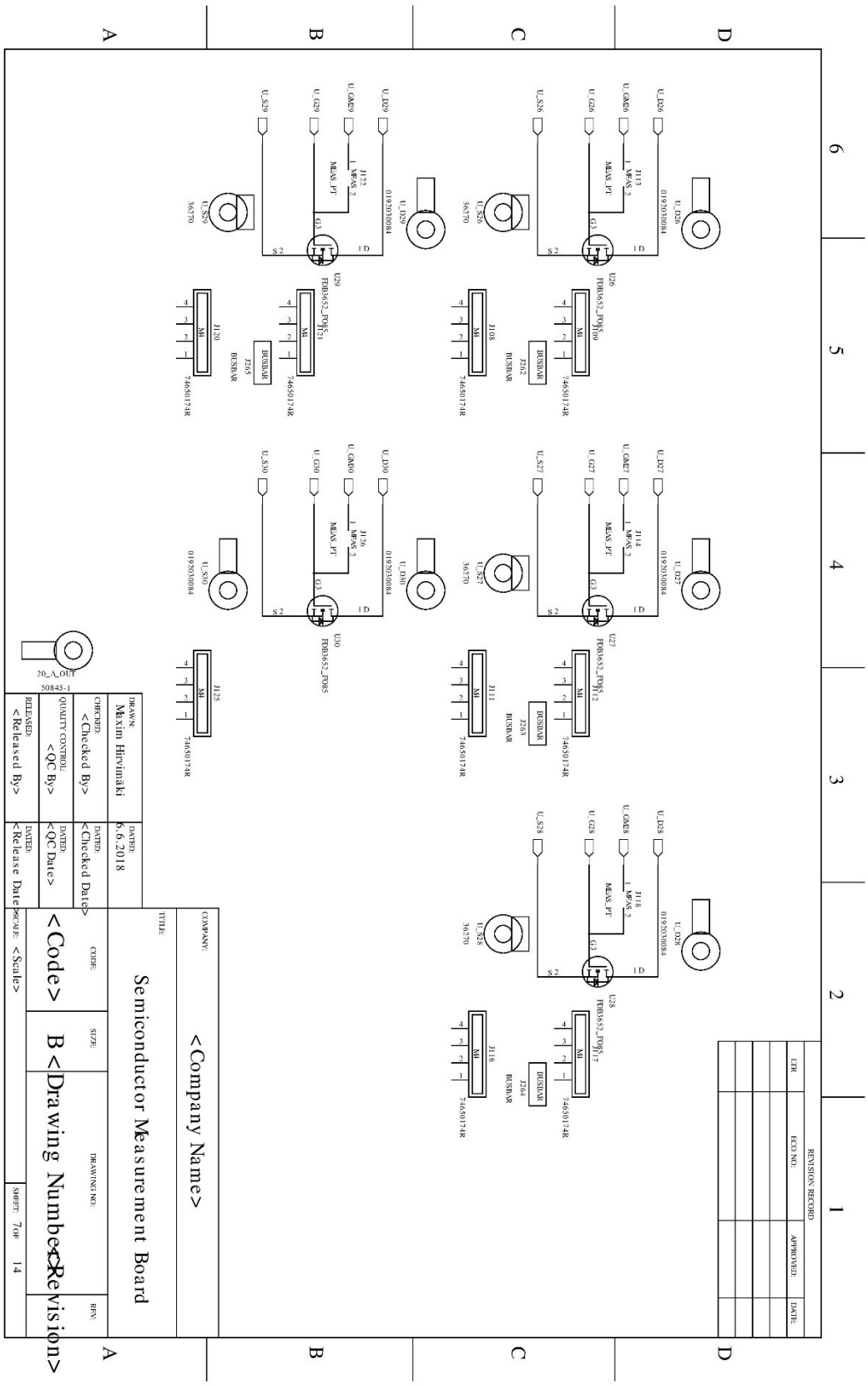


Figure A. 7 Semiconductor Measurement Board Schematic page 7

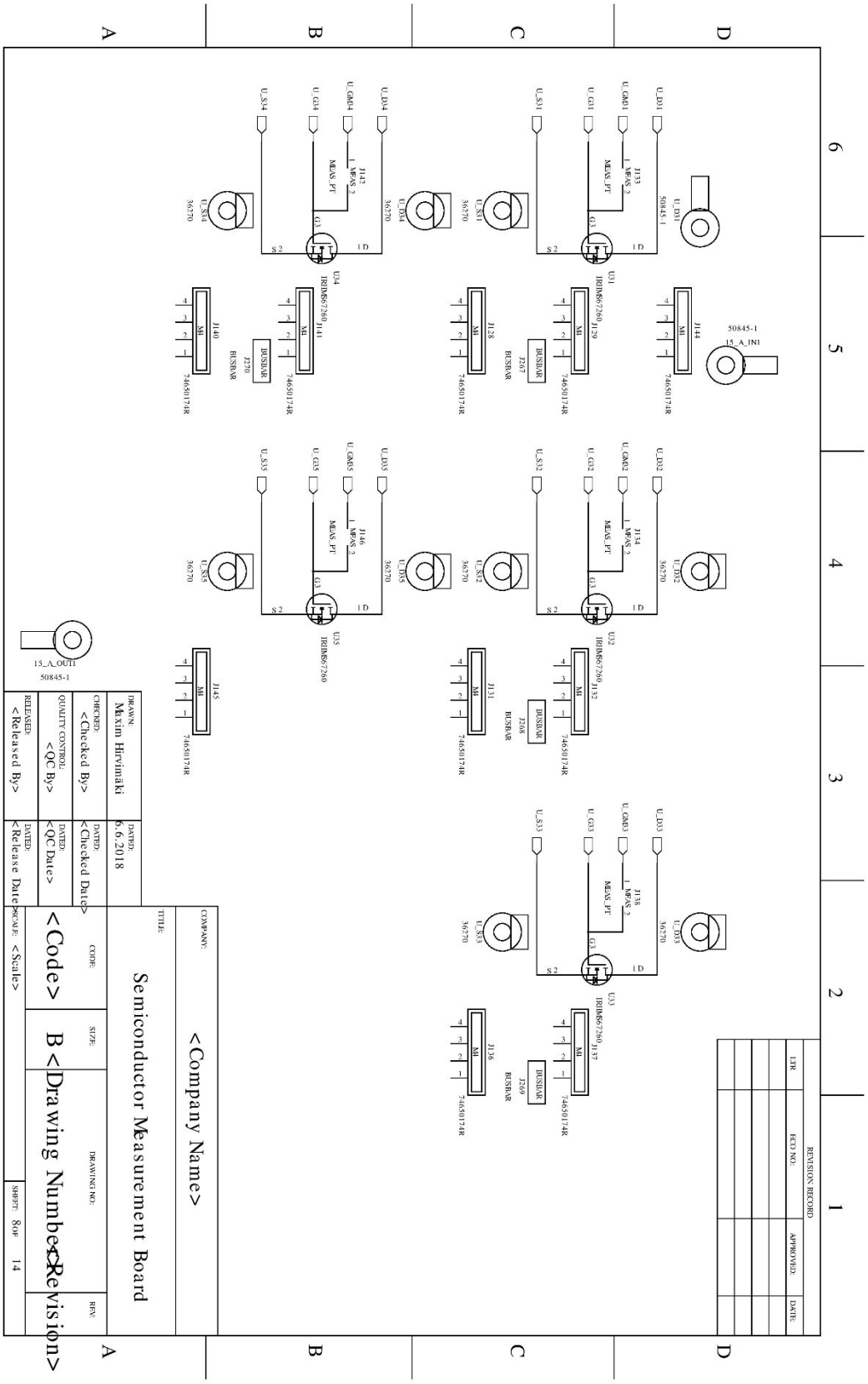


Figure A. 8 Semiconductor Measurement Board Schematic page 8

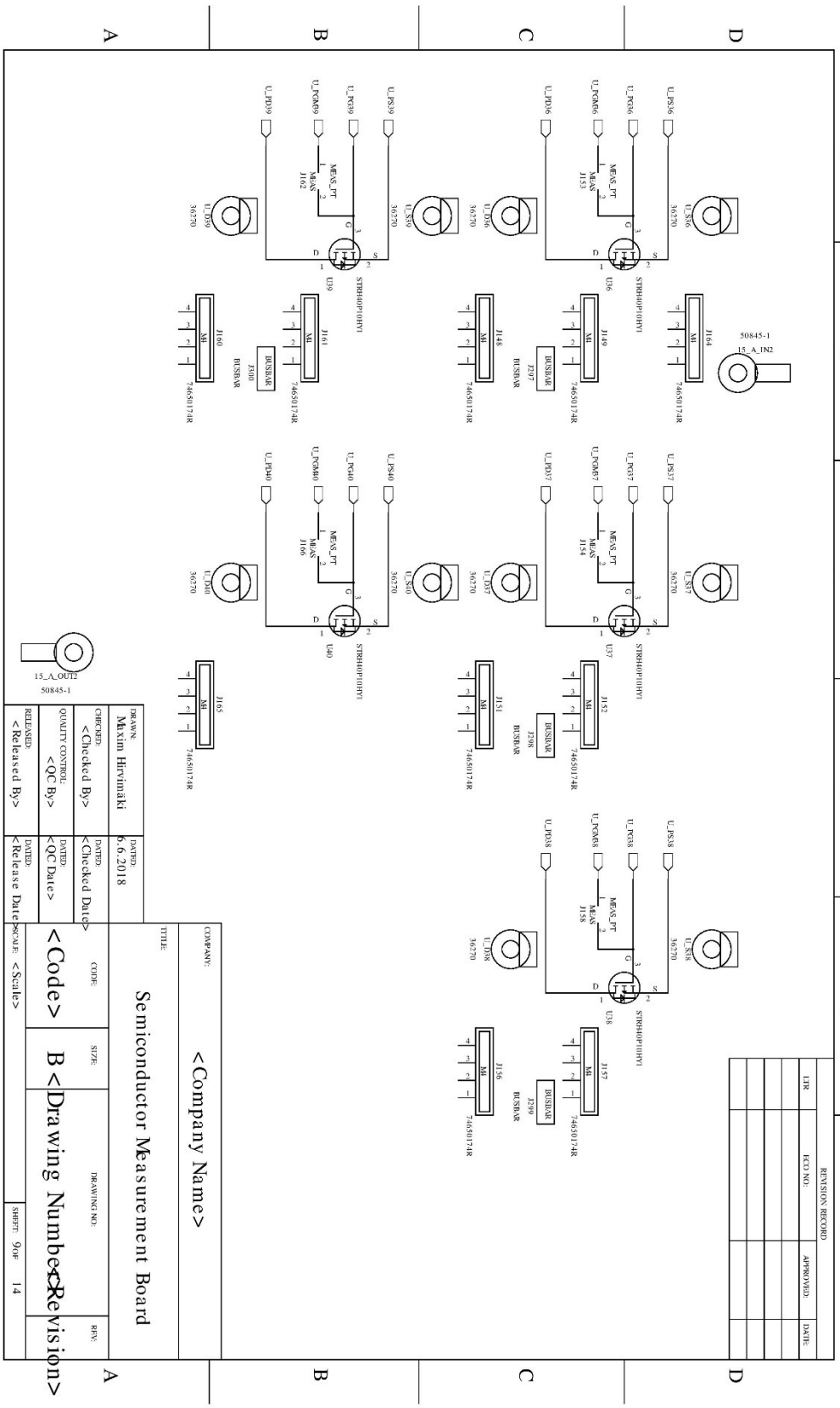


Figure A. 9 Semiconductor Measurement Board Schematic page 9

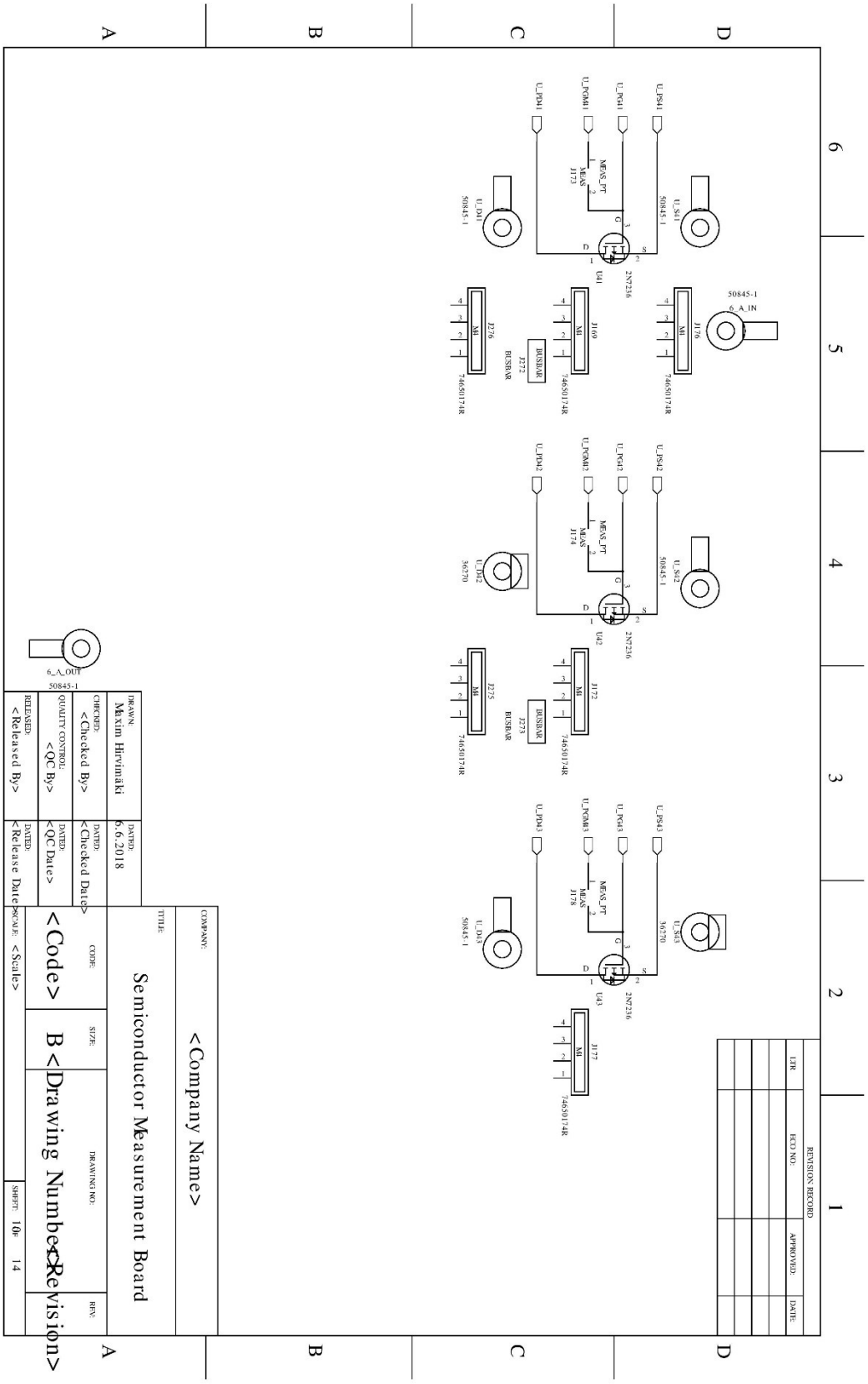


Figure A. 10 Semiconductor Measurement Board Schematic page 10

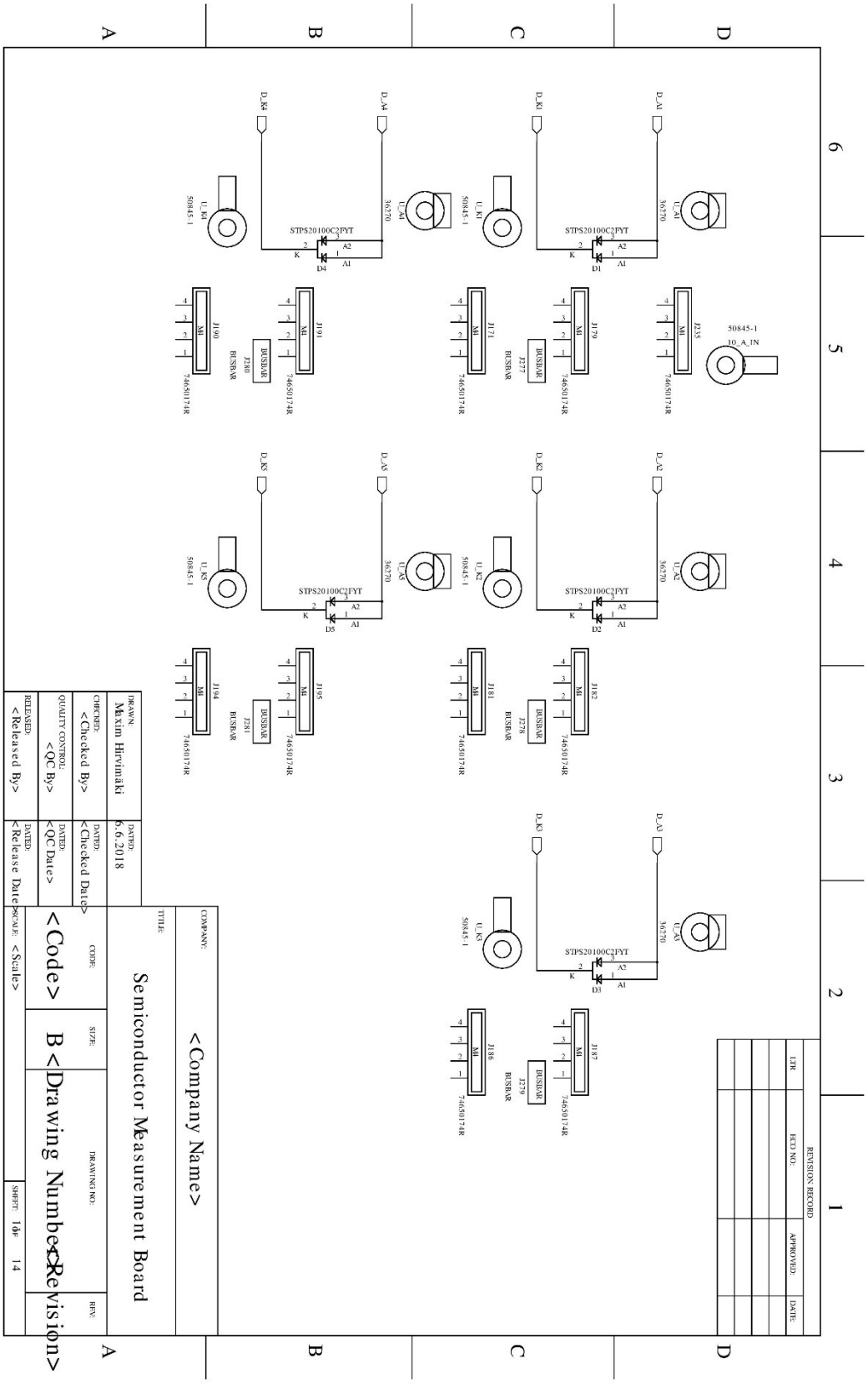


Figure A. 11 Semiconductor Measurement Board Schematic page 11

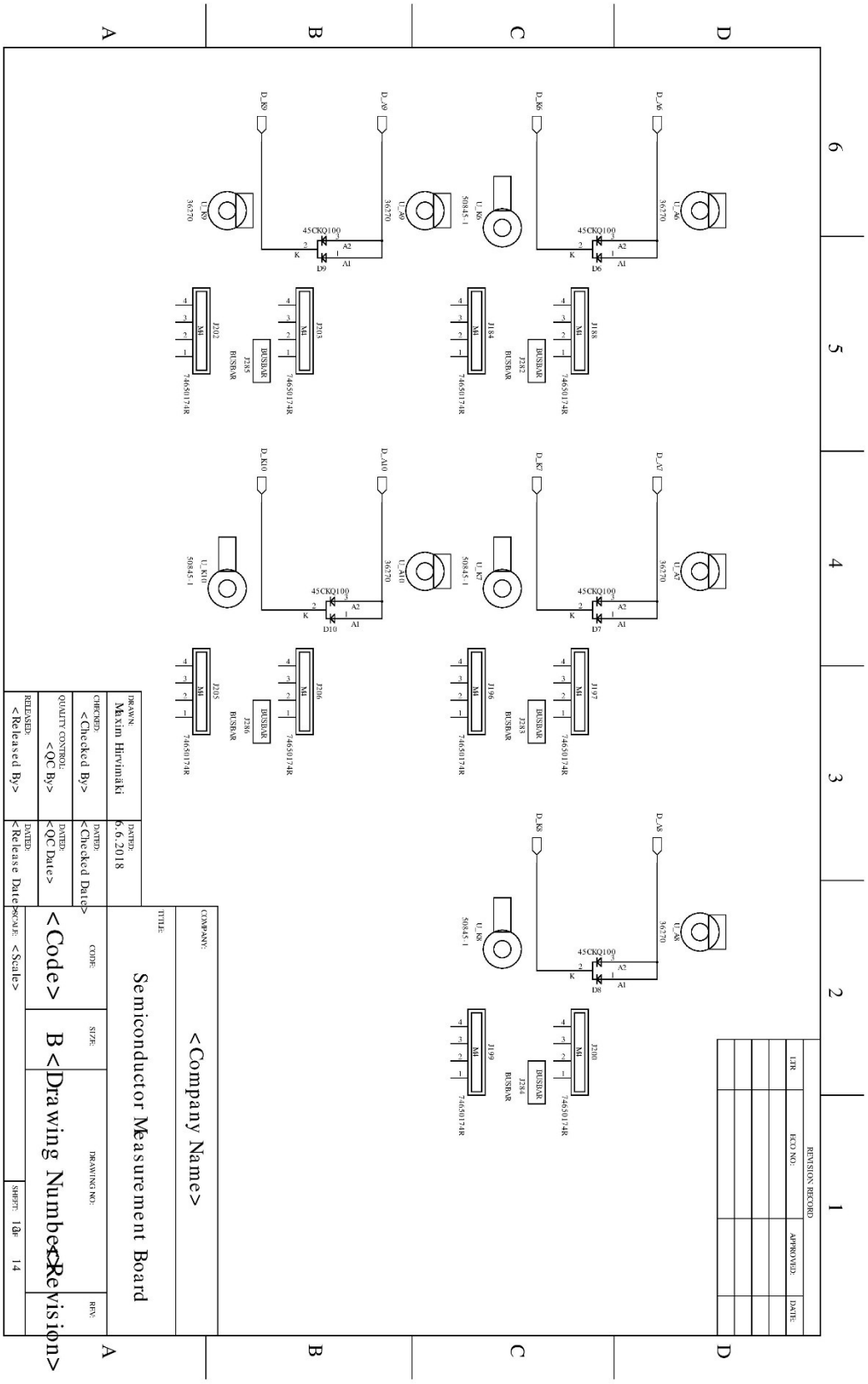


Figure A. 12 Semiconductor Measurement Board Schematic page 12

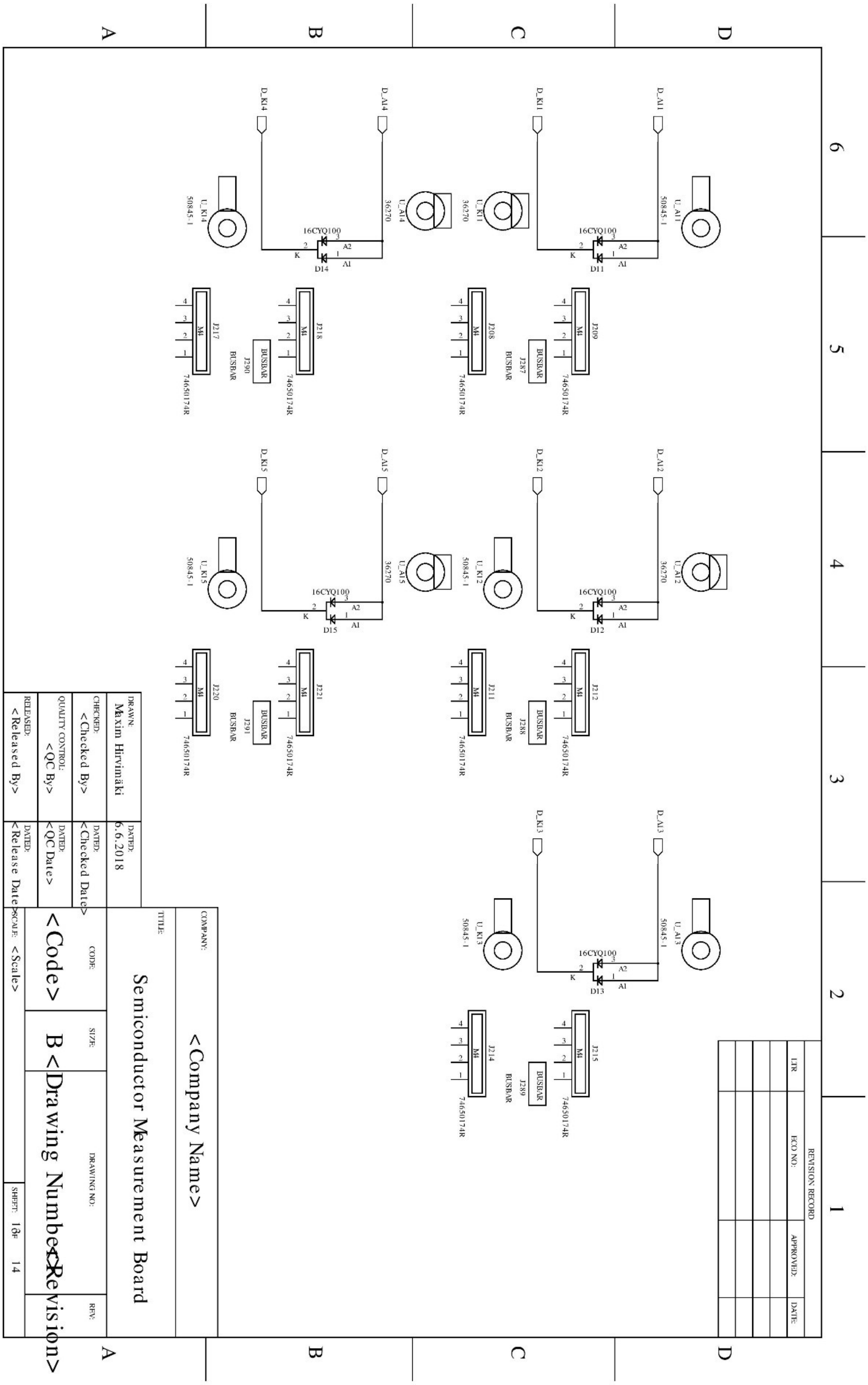


Figure A. 13 Semiconductor Measurement Board Schematic page 13

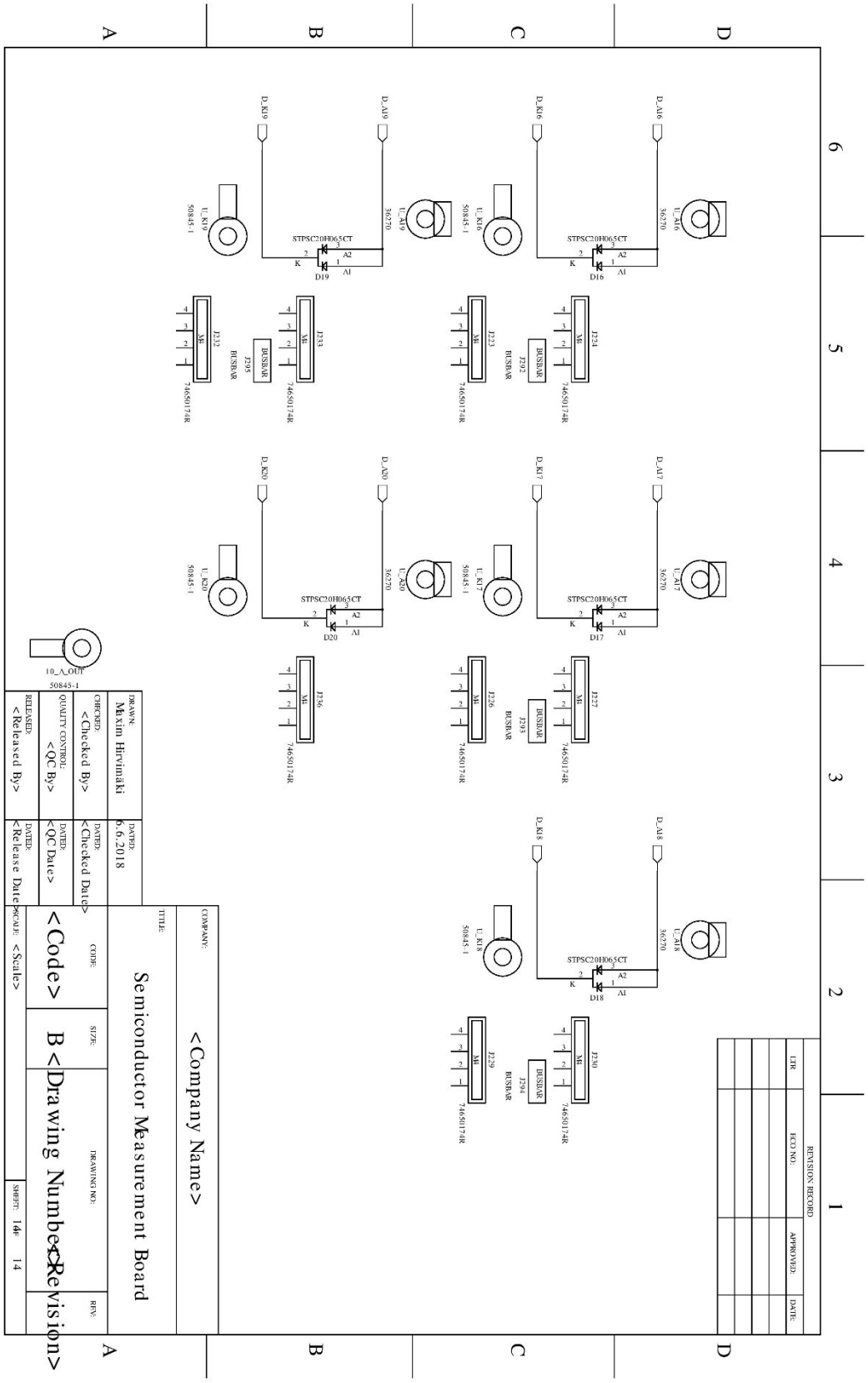


Figure A. 14 Semiconductor Measurement Board Schematic page 14

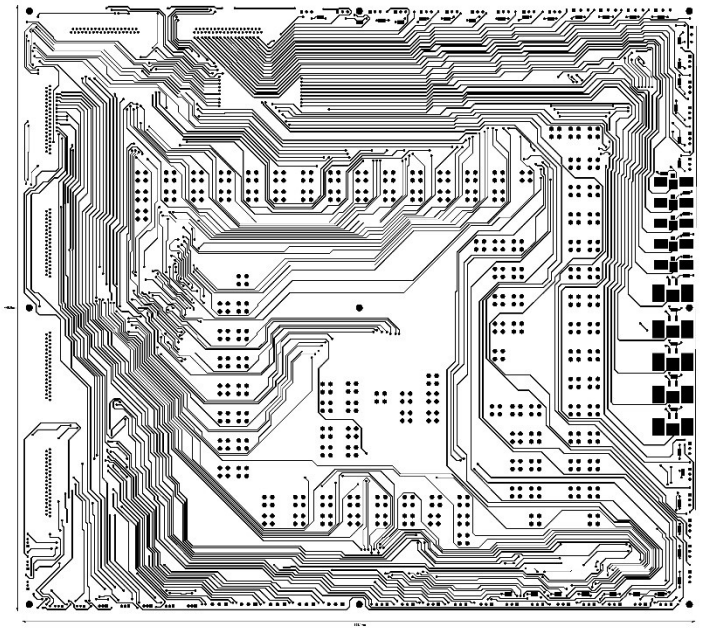


Figure A. 15 Semiconductor Measurement Board PCB Mask Top

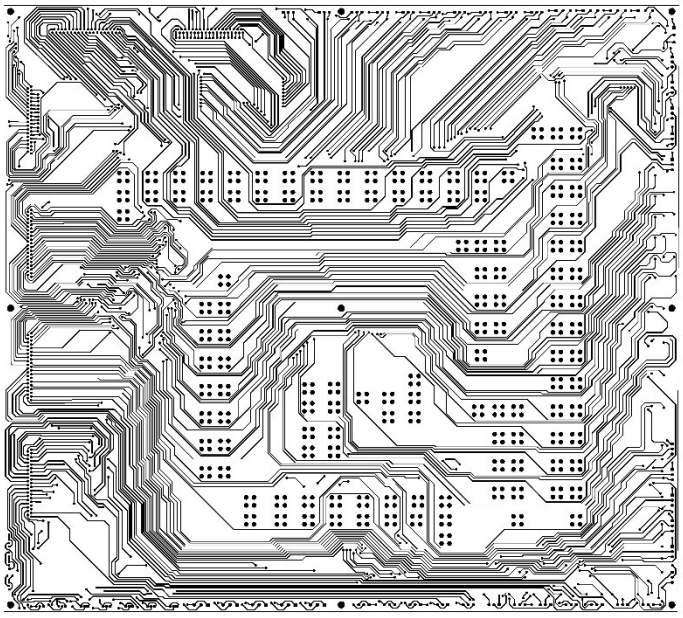


Figure A. 16 Semiconductor Measurement Board PCB Mask Bottom

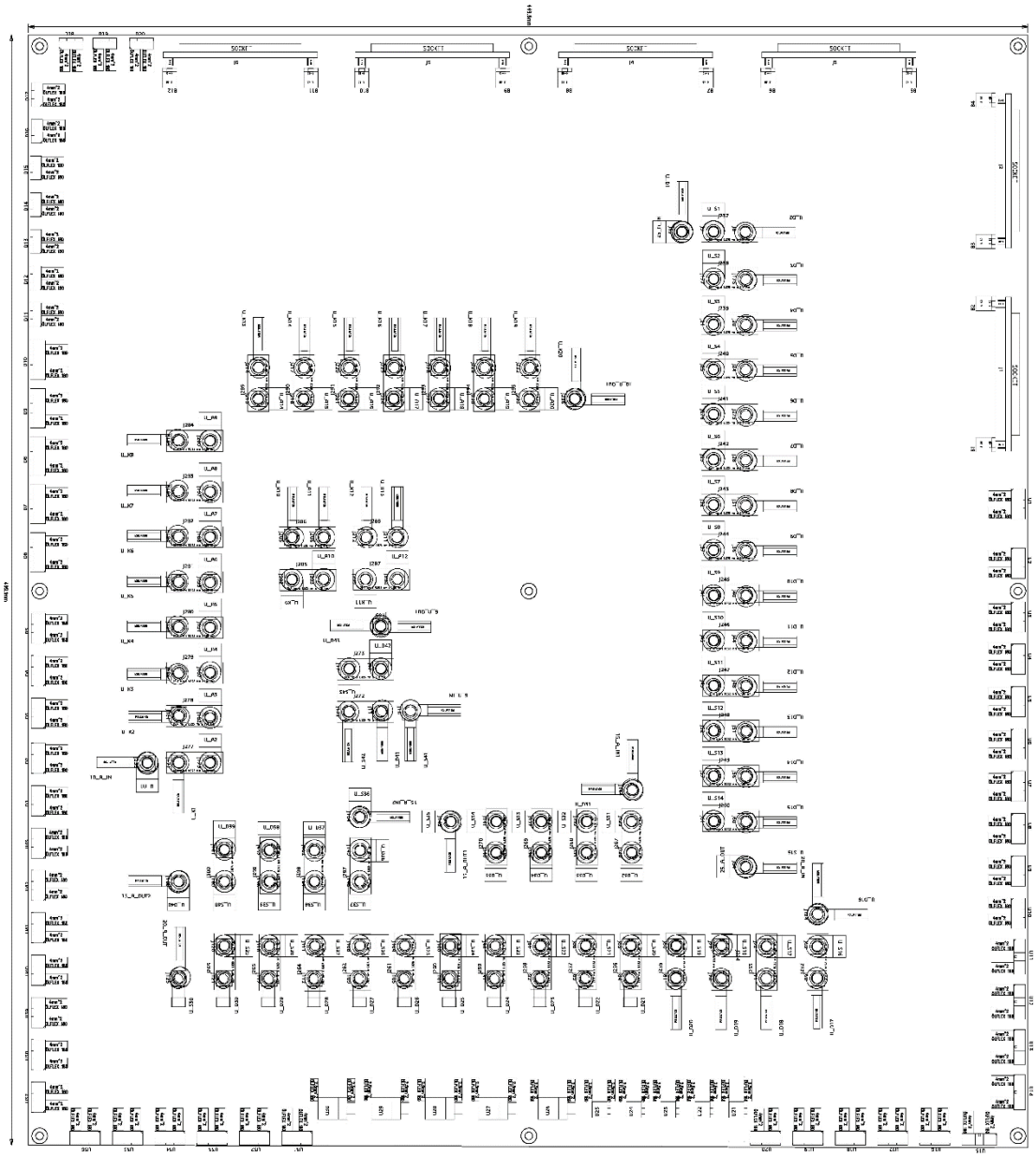


Figure A. 17 Semiconductor Measurement Board Assembly diagram. PCB size 450 mm x 500 mm

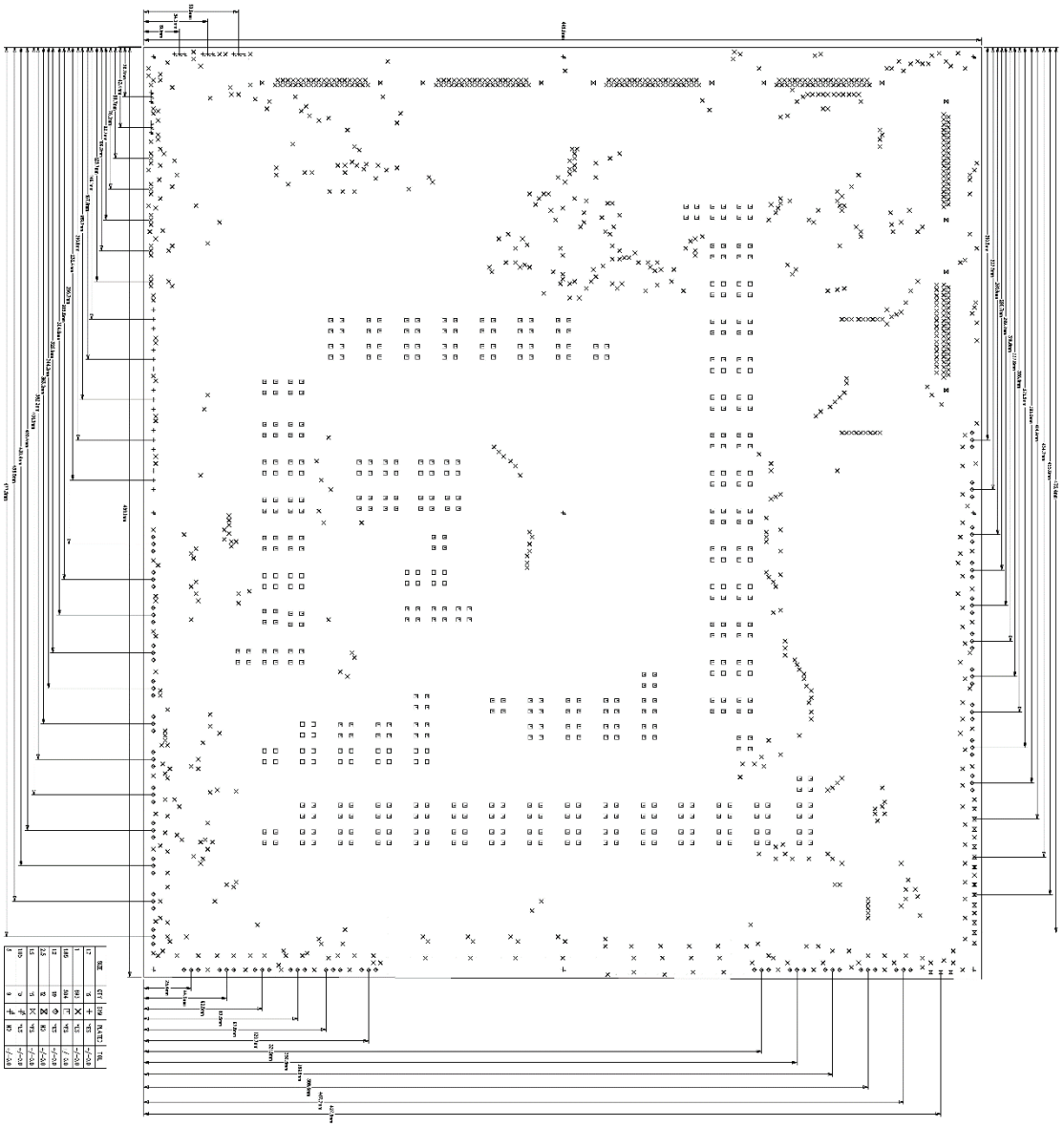


Figure A. 18 Semiconductor Measurement Board Drill diagram

Table A. 1 Reference designators and descriptions of the components used in Semiconductor Measurement Board

Ref-Des	Part Name	Desc
B1-12	621	4-40 Threaded Mounting Bracket
25_A_IN,25_A_OUT,U_A1-10,U_A12,U_A14-20,U_D32-40,U_D42,U_K9,U_K11,U_S1-14,U_S16-29,U_S31-40,U_S43	36270	Ring Terminal Connector 8 Stud Circular 10-12 AWG Crimp, Flag
U_D21-30,U_S30	0192030084	Ring Terminal Connector 8 Stud Circular 14-16 AWG Crimp
J1-6	1731090068	37 Pin, Female Socket, SIze 4 (DC,C),D-Sub Connector, Through Hole, Right Angle
D11-15	16CYQ100	SCHOTTKY RECTIFIER, HIGH EFFICIENCY SERIES Aerospace 1 x 20 and 2 x 20 A - 100 V Schottky rectifier
U41-43	2N7236	P-CHANNEL POWER MOSFET THRU-HOLE
D6-10	45CKQ100	SCHOTTKY RECTIFIER, HIGH EFFICIENCY SERIES Aerospace 1 x 20 and 2 x 20 A - 100 V Schottky rectifier

10_A_IN,10_A_OUT,15_A_IN1-2,15_A_OUT1-2,20_A_IN,20_A_OUT,6_A_IN,6_A_OUT,U_A11,U_A13,U_D1-20,U_D31,U_D41,U_D43,U_K1-8,U_K10,U_K12-20,U_S15,U_S41-42	50845-1	CONN RING CIRC 10-12AWG #8 CRIMP
J8-9,J11-12,J16-17,J20-21,J24-25,J28-29,J31-32,J36-37,J40-41,J44-45,J48-49,J51-52,J56-57,J60-61,J64-65,J68-69,J71-72,J76-77,J80-81,J84-85,J88-89,J91-92,J96-97,J100-101,J104-105,J108-109,J111-112,J116-117,J120-121,J124-125,J128-129,J131-132,J136-137,J140-141,J144-145,J148-149,J151-152,J156-157,J160-161,J164-165,J169,J171-172,J176-177,J179,J181-182,J184,J186-188,J190-191,J194-197,J199-200,J202-203,J205-206,J208-209,J211-212,J214-215,J217-218,J220-221,J223-224,J226-227,J229-230,J232-233,J235-236,J275-276	74650174R	4 Pin Screw Terminal, Power Tap M4 Through Hole
J237-250,J252-265,J267-270,J272-273,J277-295,J297-300	BUSBAR	25.4mm x 9.525mm x 1.09mm Solid Copper Busbar with two 5mm holes (pitch 14.30mm)
U26-30	FDB3652_FO85	N-Channel PowerTrench MOSFET
U1-5	IRHMS57160	N-CHANNEL RADIATION HARDENED POWER MOSFET THRU-HOLE
U31-35	IRHMS67260	N-CHANNEL RADIATION HARDENED POWER MOSFET THRU-HOLE
U6-10	JANSR2N7470T1	N-CHANNEL RADIATION HARDENED POWER MOSFET THRU-HOLE
J13-14,J18,J22,J26,J33-34,J38,J42,J46,J53-54,J58,J62,J66,J73-74,J78,J82,J86,J93-94,J98,J102,J106,J113-114,J118,J122,J126,J133-134,J138,J142,J146,J153-154,J158,J162,J166,J173-174,J178	MEAS_PT	Separate path for measurements
U11-15	SCTW100N65G2AG	Automotive silicon carbide Power MOSFET
U21-25	SQJ402EP	Automotive N-Channel 100 V (D-S) 175 °C MOSFET
D1-5	STPS20100C2FYT	Aerospace 1 x 20 and 2 x 20 A - 100 V Aerospace 1 x 20 and 2 x 20 A - 100 V Schottky rectifier
D16-20	STPSC20H065CT	SCHOTTKY RECTIFIER, HIGH EFFICIENCY SERIES650 V power Schottky silicon carbide diode
U16-20	STRH100N10HY1	Rad-Hard N-Channel 100V - 48A MOSFET
U36-40	STRH40P10HY1	Rad-Hard P-Channel 100 V - 40A MOSFET
NON-PCB		
Reference	**Length total per test(m)**	**Description**
ÖLFLEX HEAT 180 6mm^2	60	Wires from loads or High Current Power Supply that enter the thermal chamber
ÖLFEX HEAT 180 4mm^2	35	Interconnections from transistor D + S and diode A + K to busbars
ÖLFLEX HEAT 180 2.5mm^2	8	Interconnections from surface mount transistor D + S
ÖFLEX HEAT 180 0.50mm^2	1110	Wires for D37 connector
DCMM-37P		Cable side D37 plug that has -55 to 150 degC temperature range

APPENDIX B: SEMICONDUCTOR BREAKOUT BOX

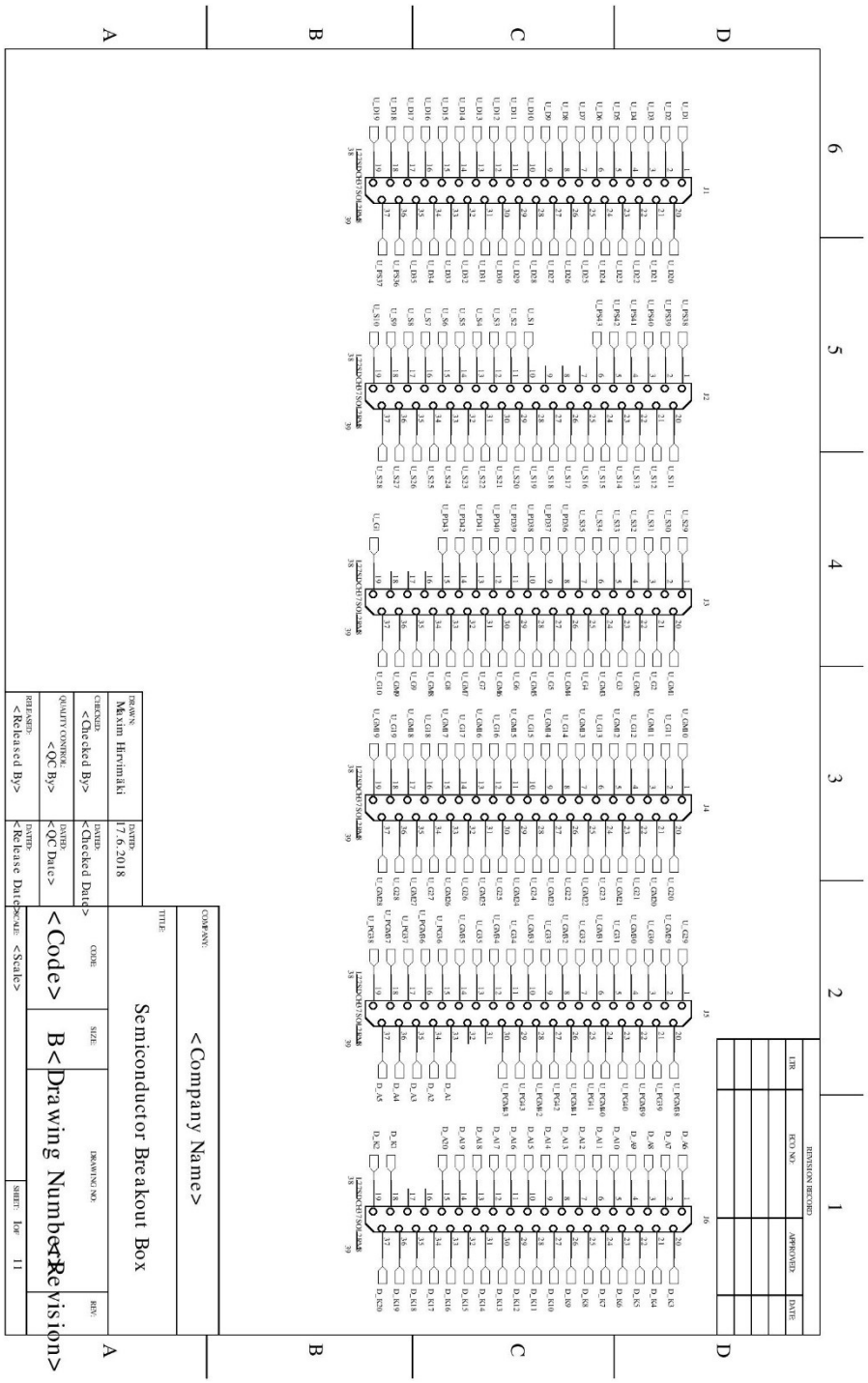


Figure B. 1 Semiconductor Breakout Box Schematic page 1

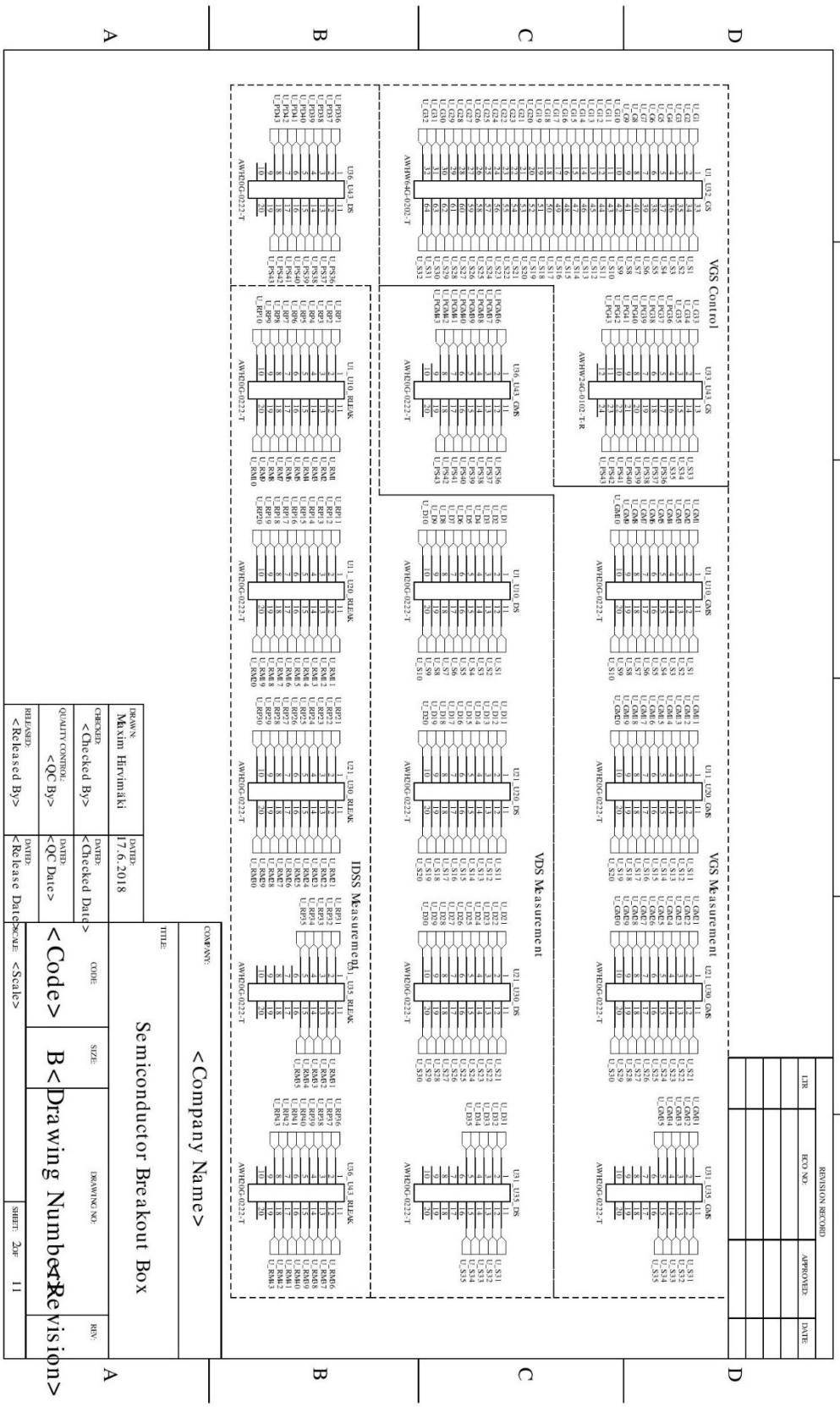


Figure B. 2 Semiconductor Breakout Box Schematic page 2

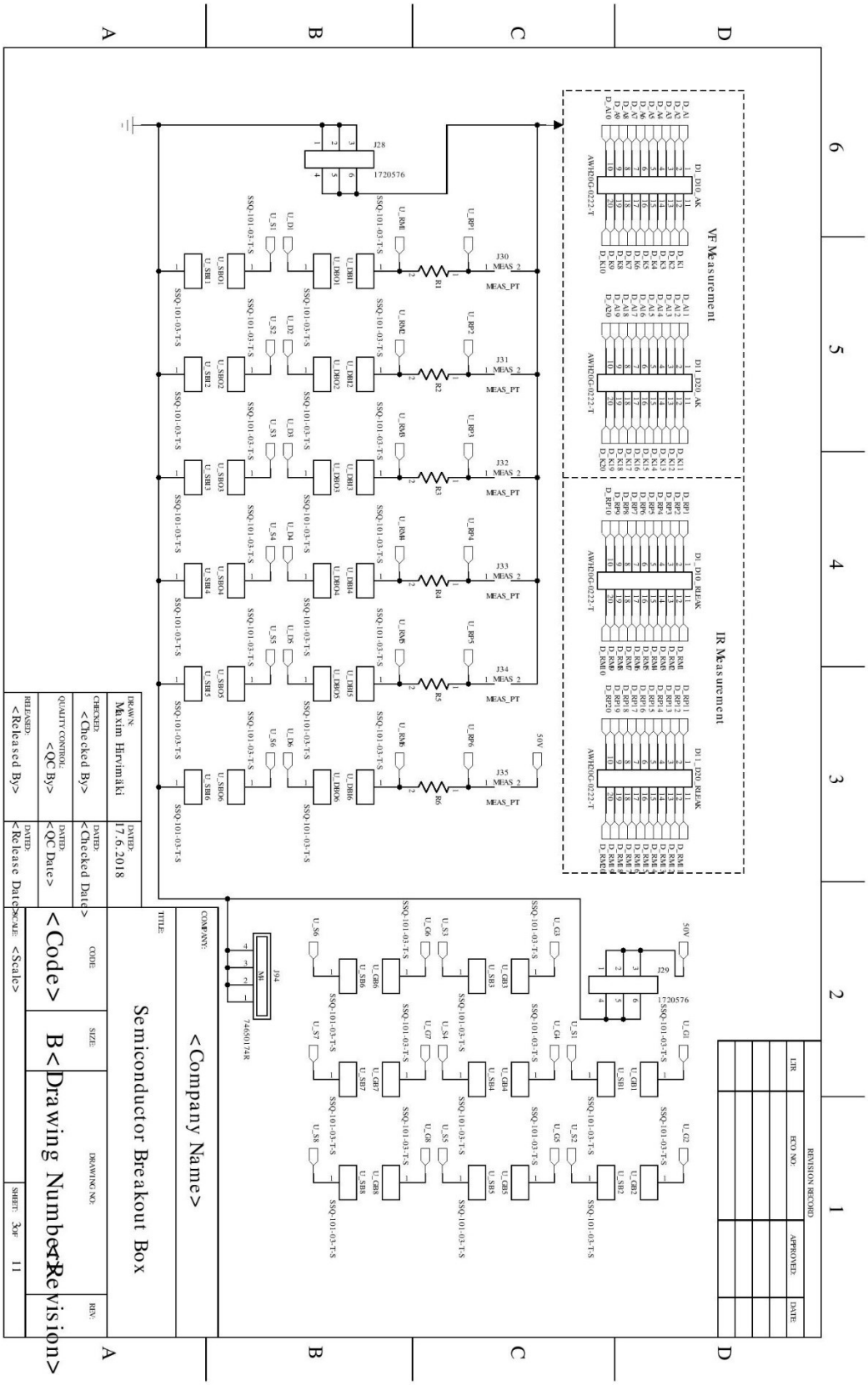


Figure B. 3 Semiconductor Breakout Box Schematic page 3

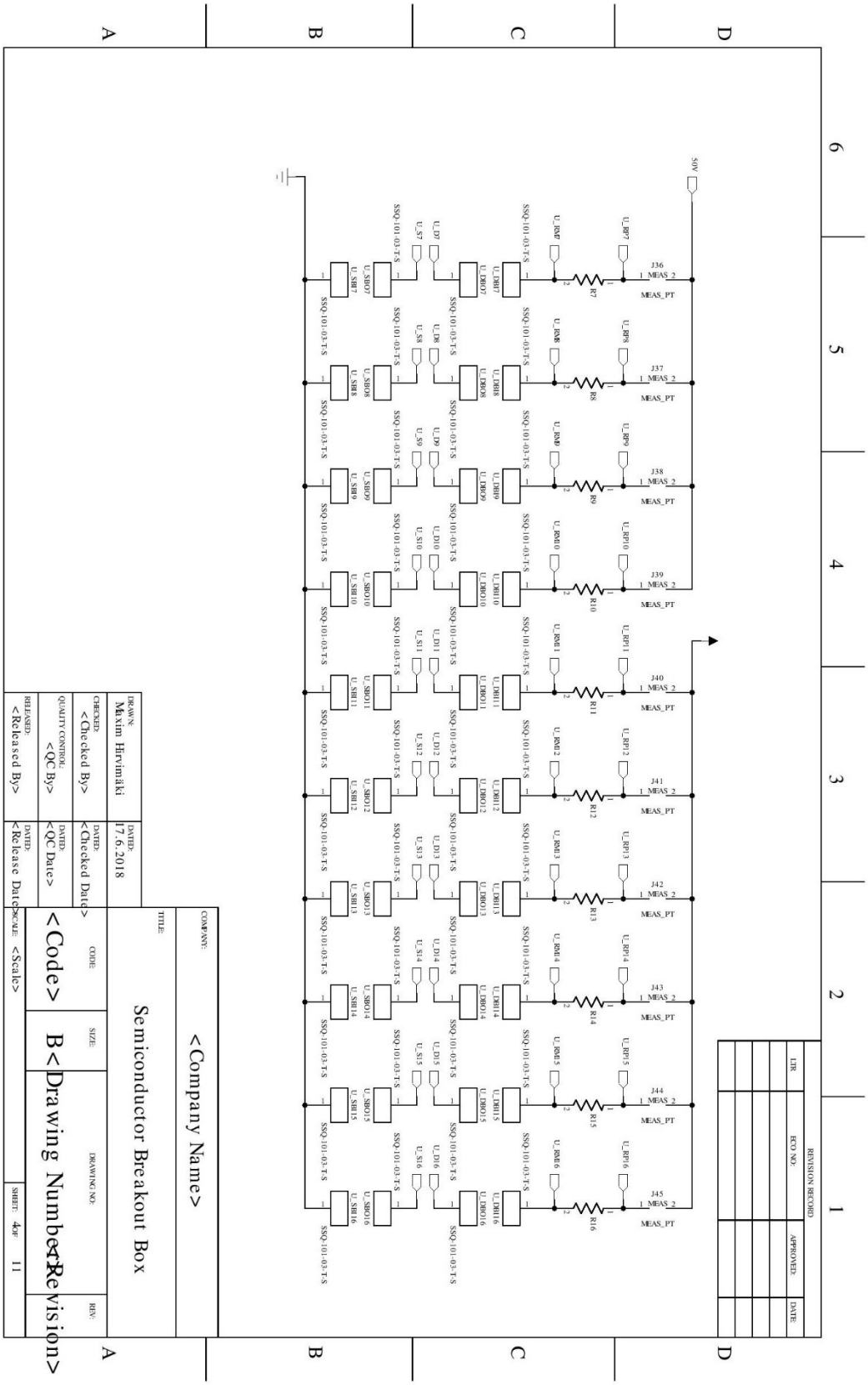


Figure B. 4 Semiconductor Breakout Box Schematic page 4

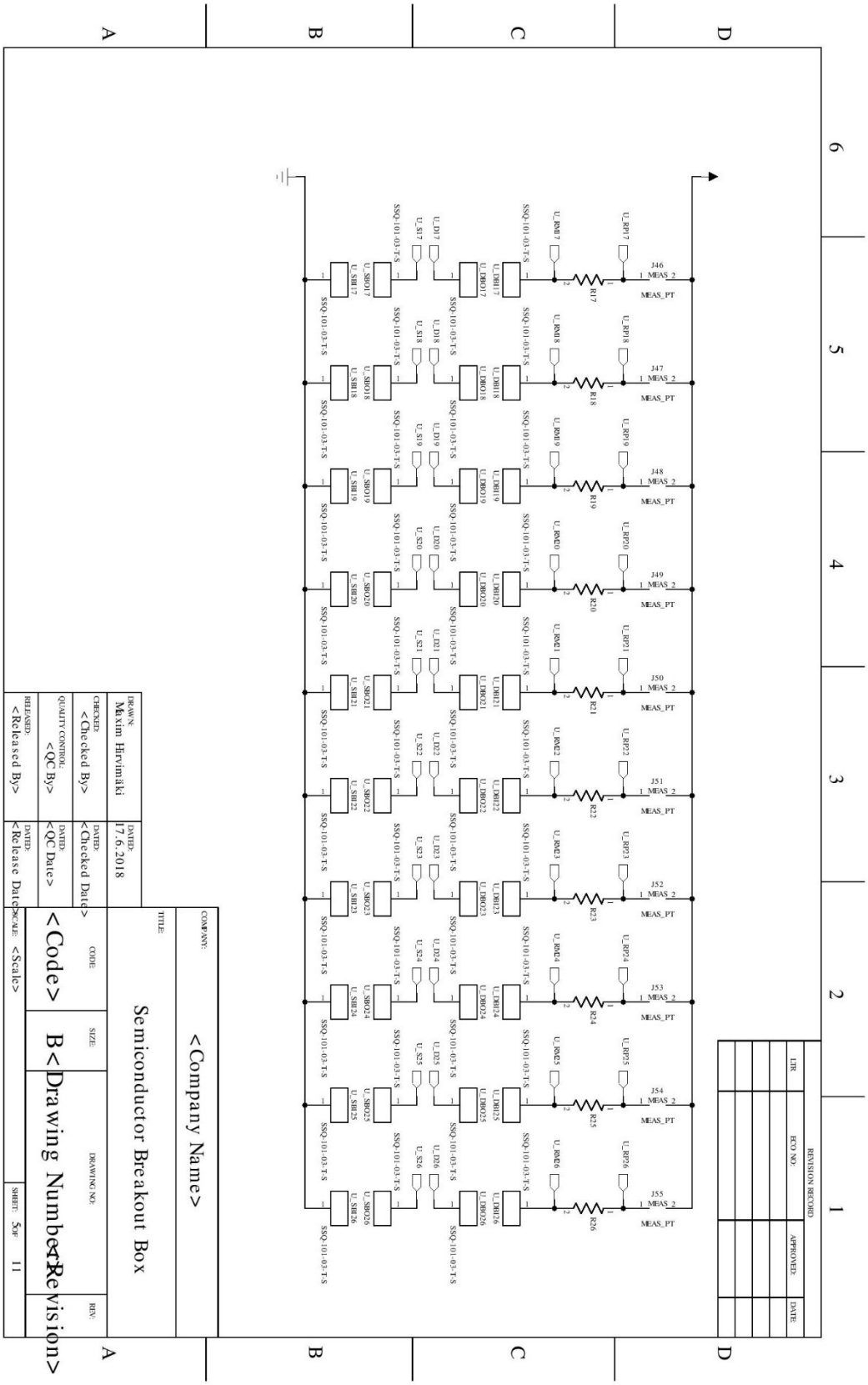


Figure B. 5 Semiconductor Breakout Box Schematic page 5

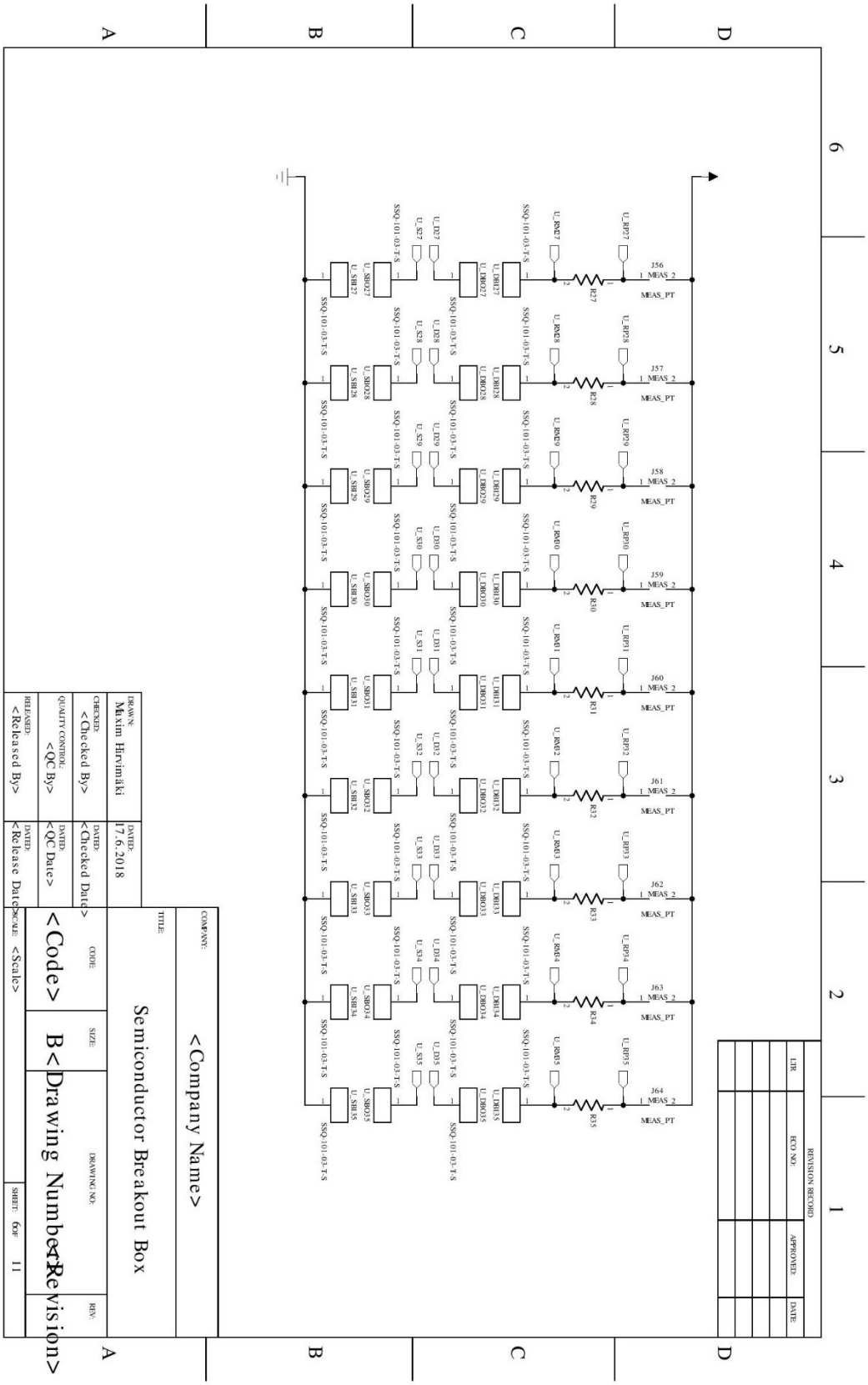


Figure B. 6 Semiconductor Breakout Box Schematic page 6

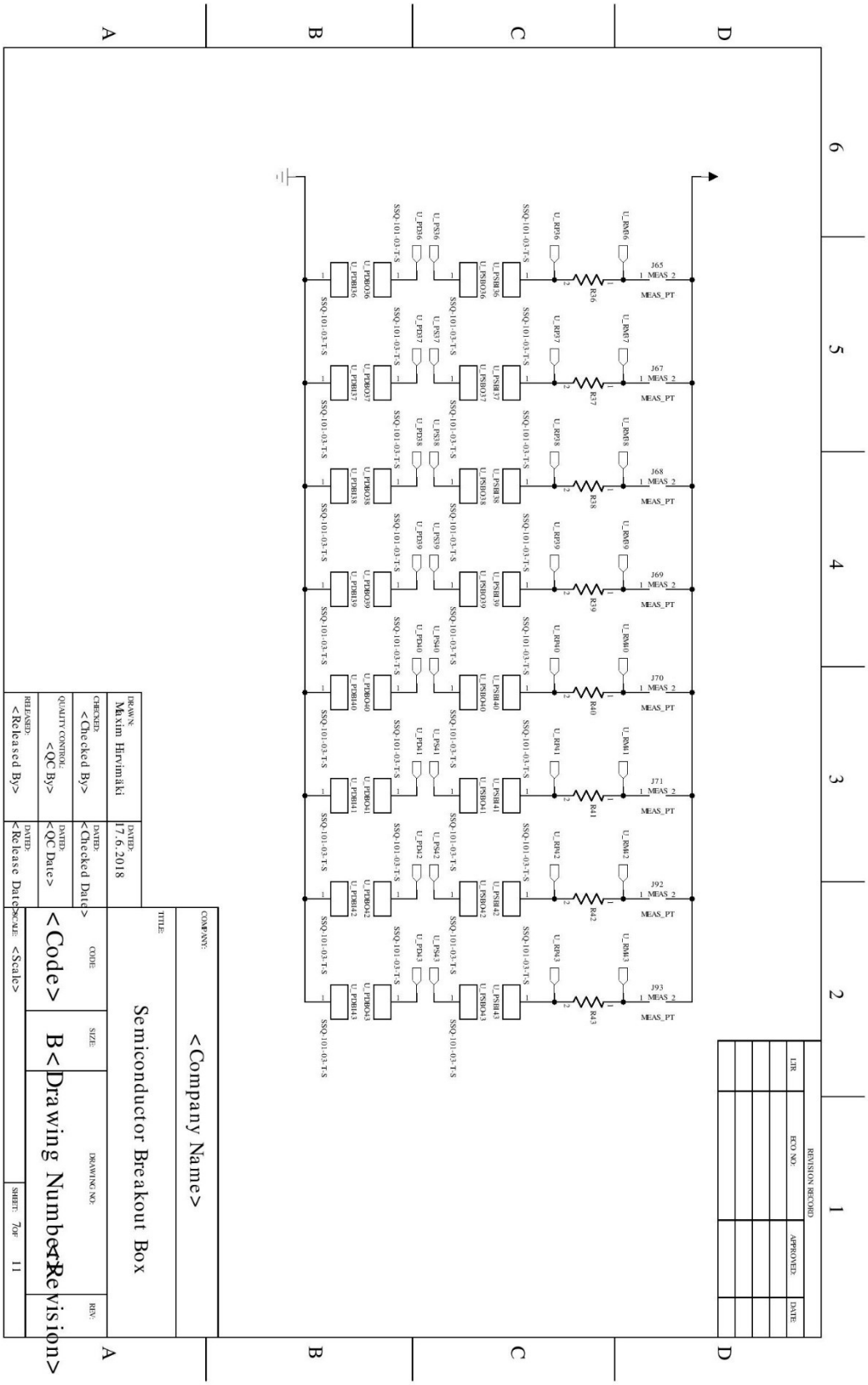


Figure B. 7 Semiconductor Breakout Box Schematic page 7

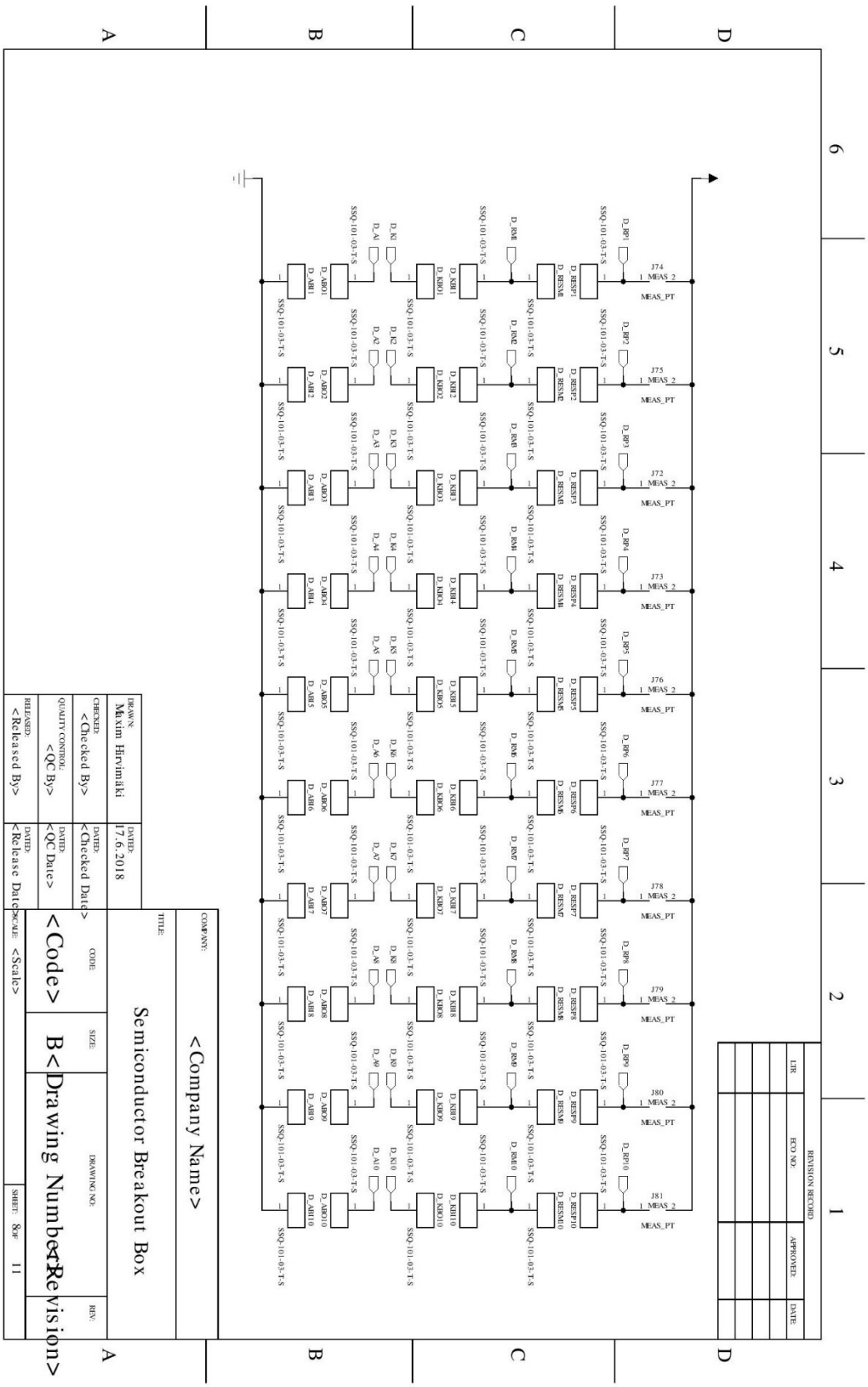


Figure B. 8 Semiconductor Breakout Box Schematic page 8

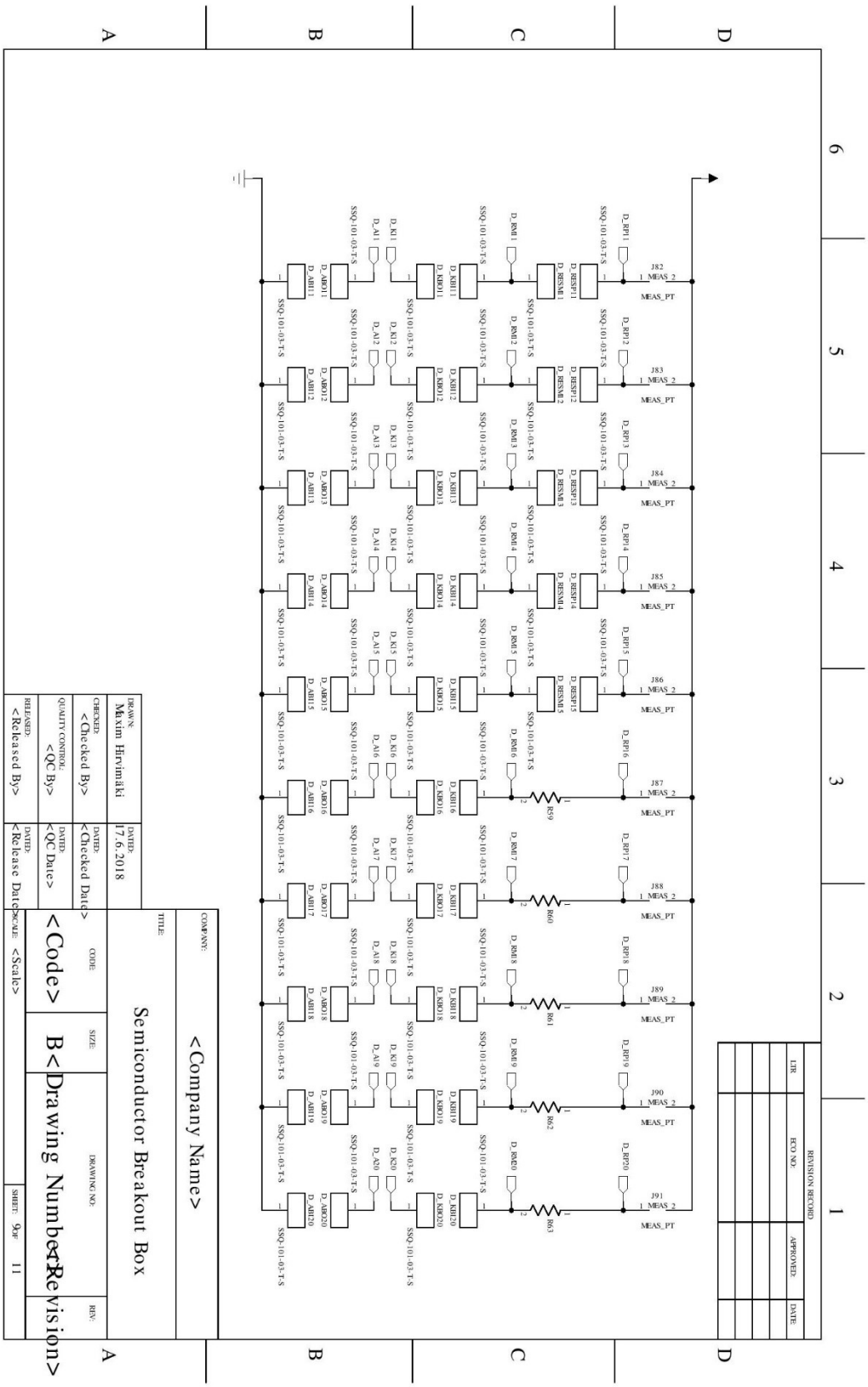


Figure B. 9 Semiconductor Breakout Box Schematic page 9

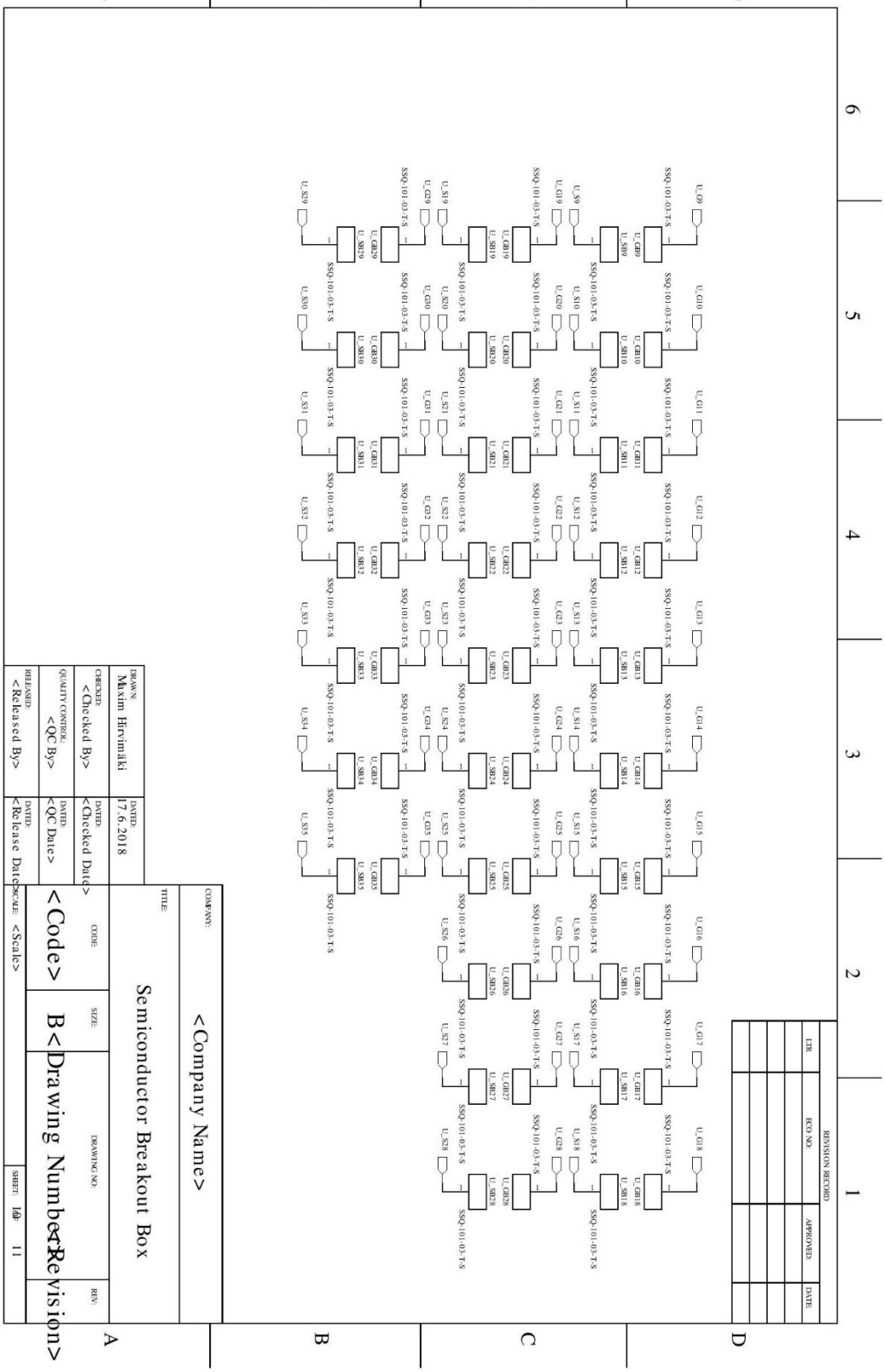


Figure B. 10 Semiconductor Breakout Box Schematic page 10

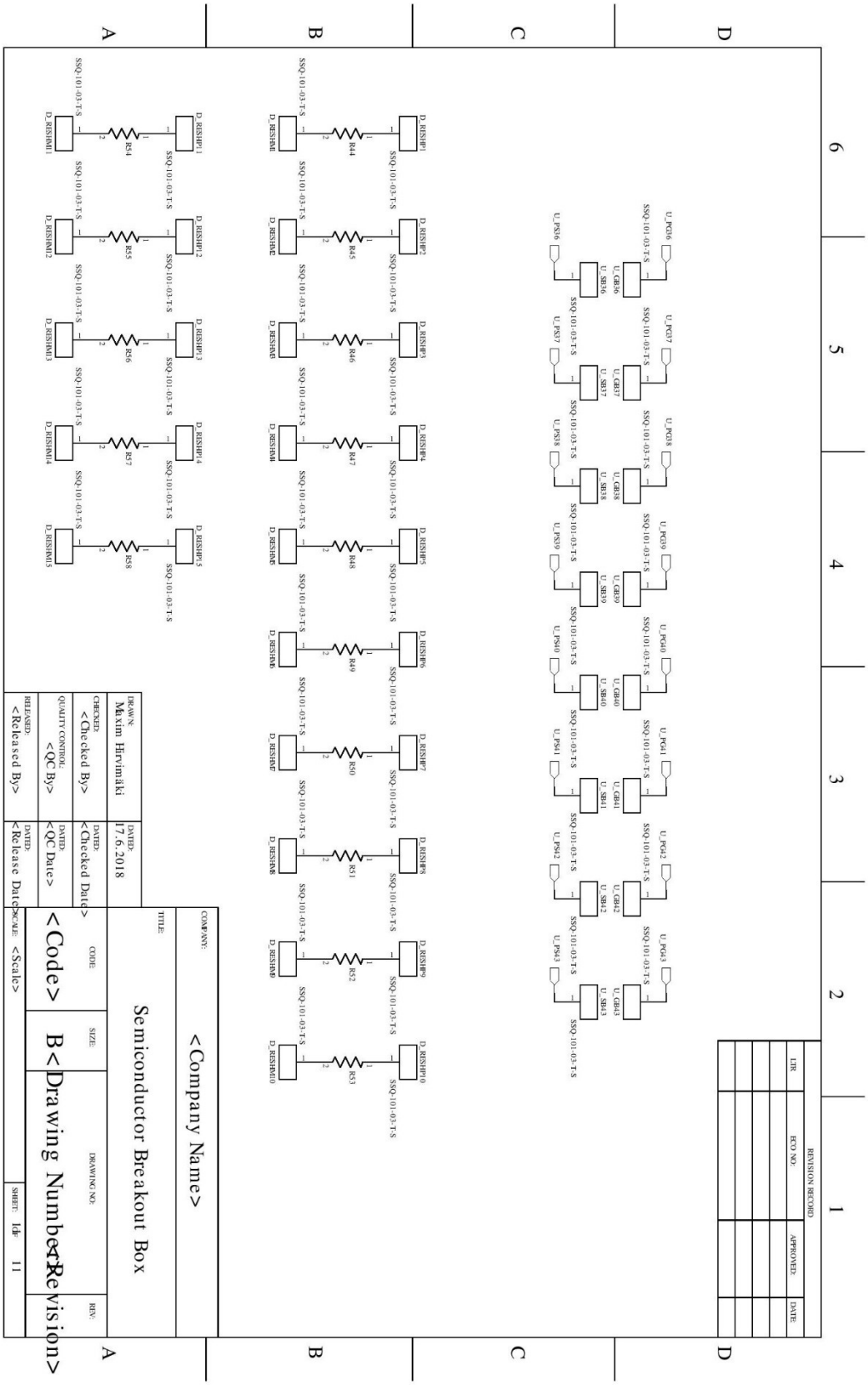


Figure B. 11 Semiconductor Breakout Box Schematic page 11

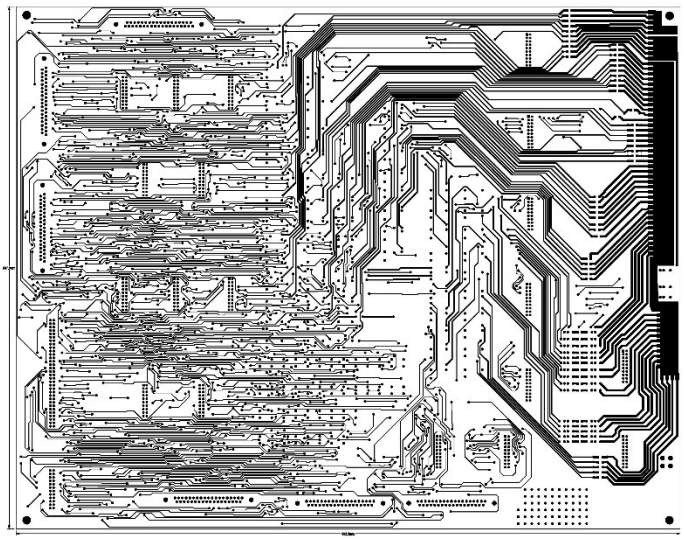


Figure B. 12 Semiconductor Breakout Box PCB Mask Top

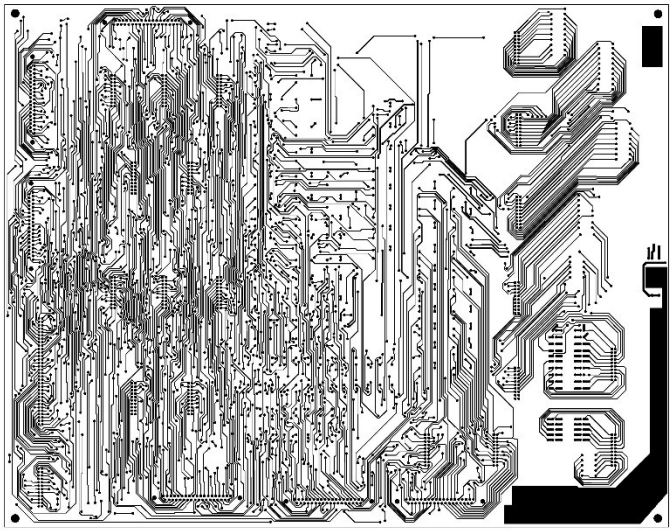


Figure B. 13 Semiconductor Breakout Box PCB Mask Bottom

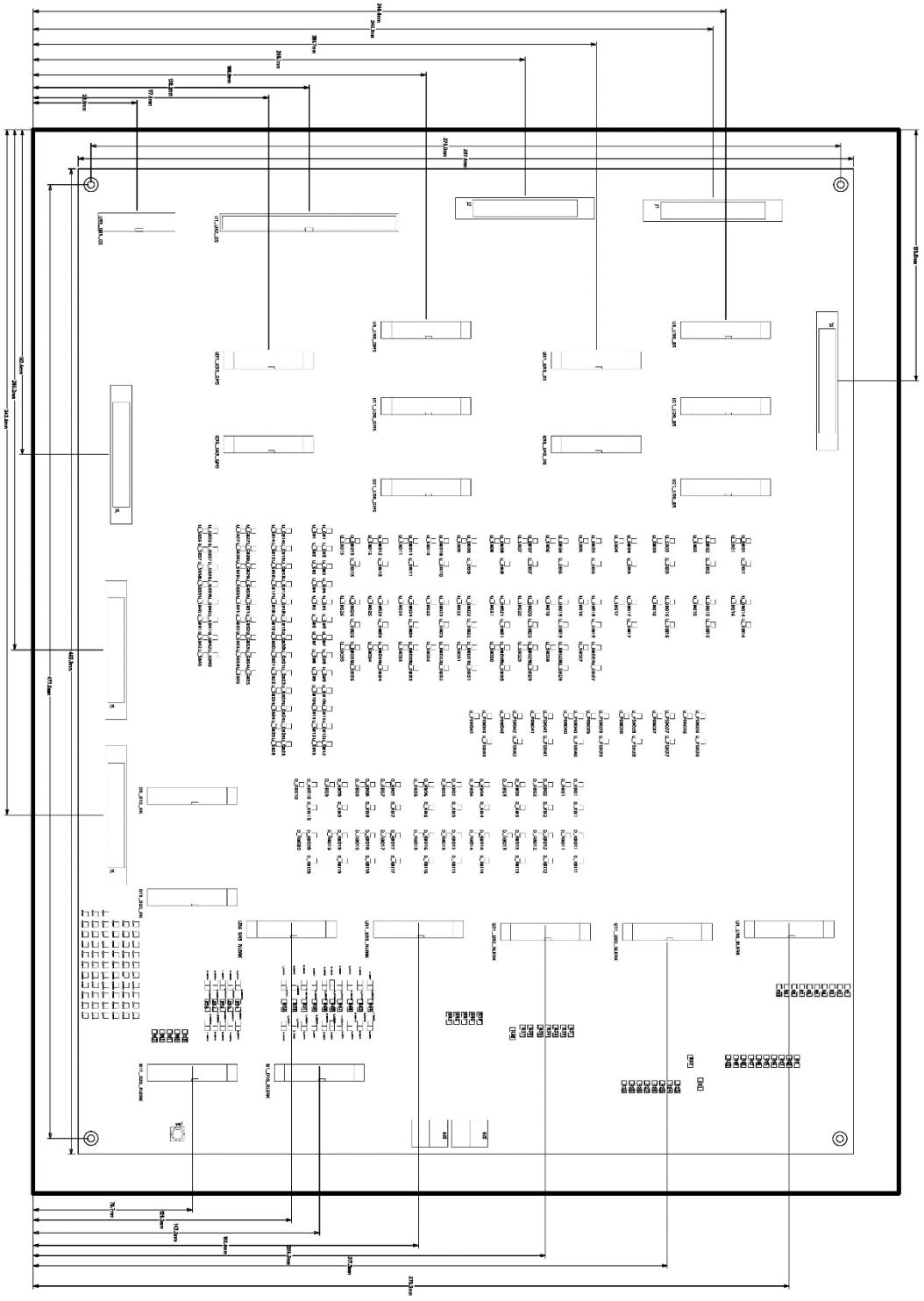


Figure B. 14 Semiconductor Breakout Box Assembly diagram. PCB size 485 mm x 390 mm

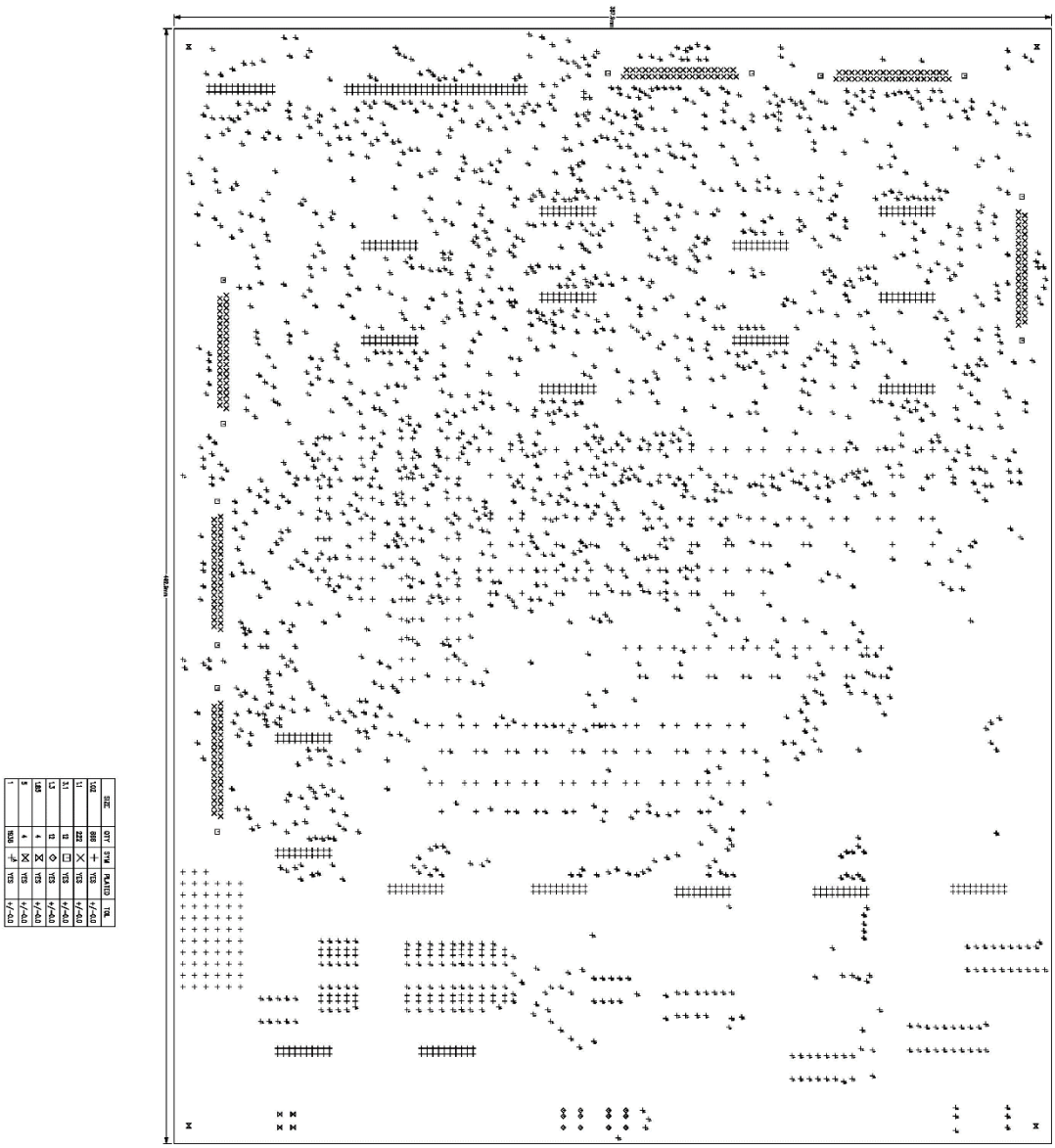


Figure B. 15 Semiconductor Breakout Box Drill diagram

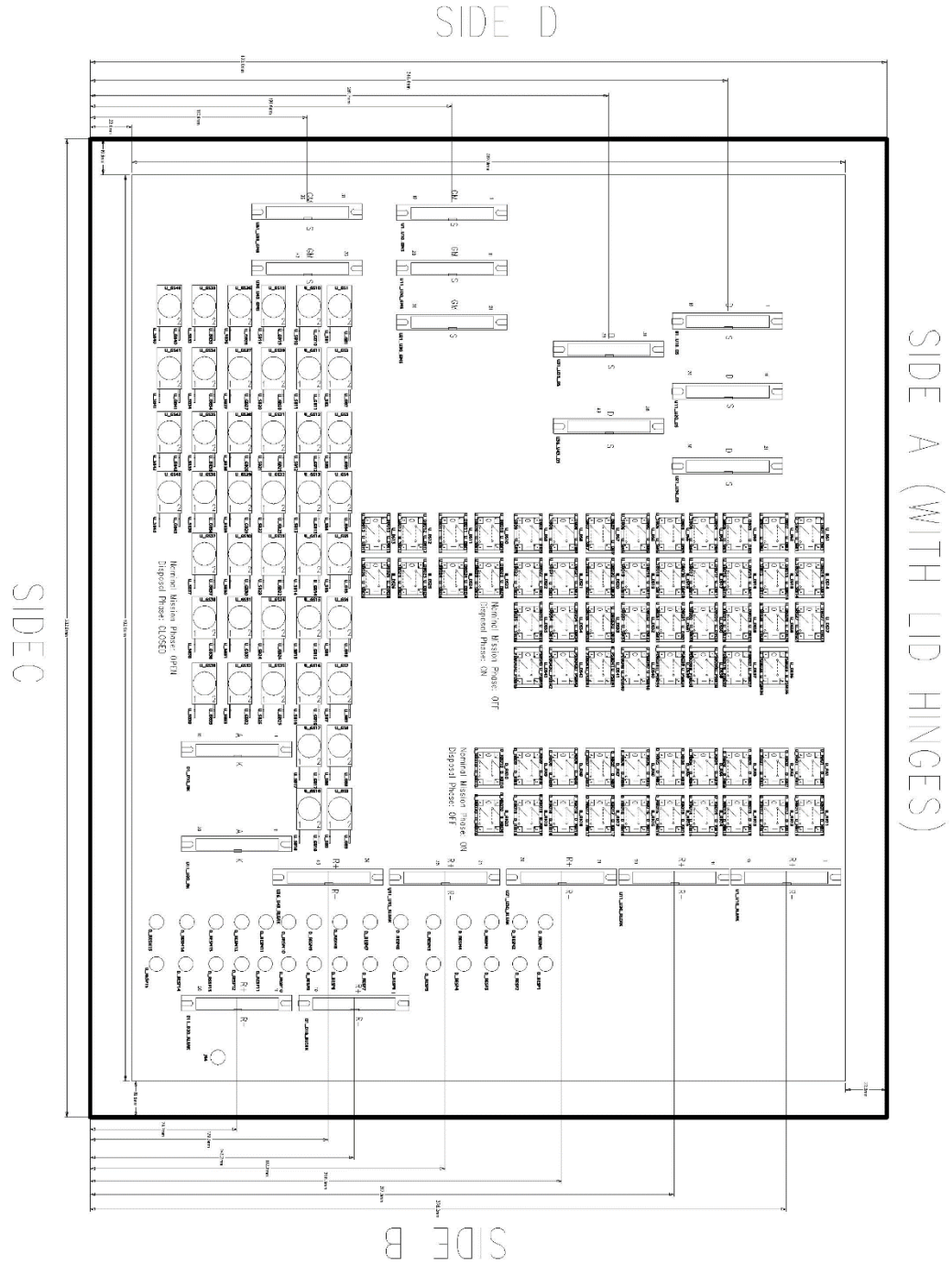


Figure B. 16 Semiconductor Breakout Box Cover Sketch

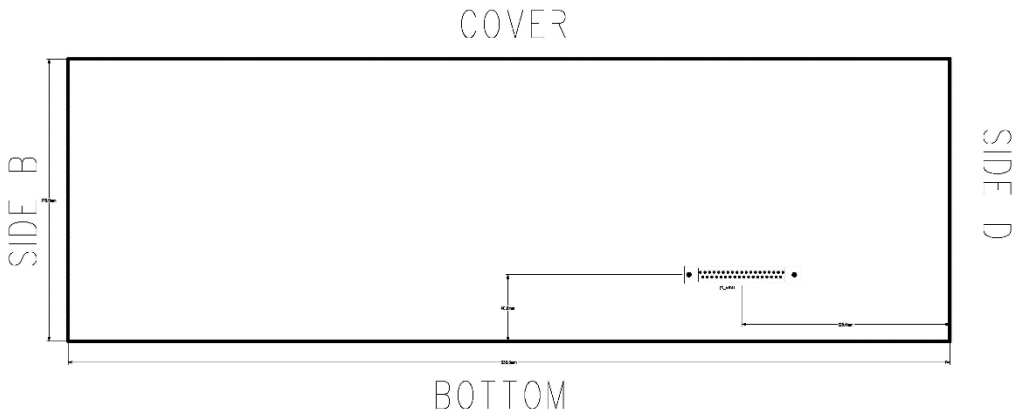


Figure B. 17 Semiconductor Breakout Box Side A Sketch

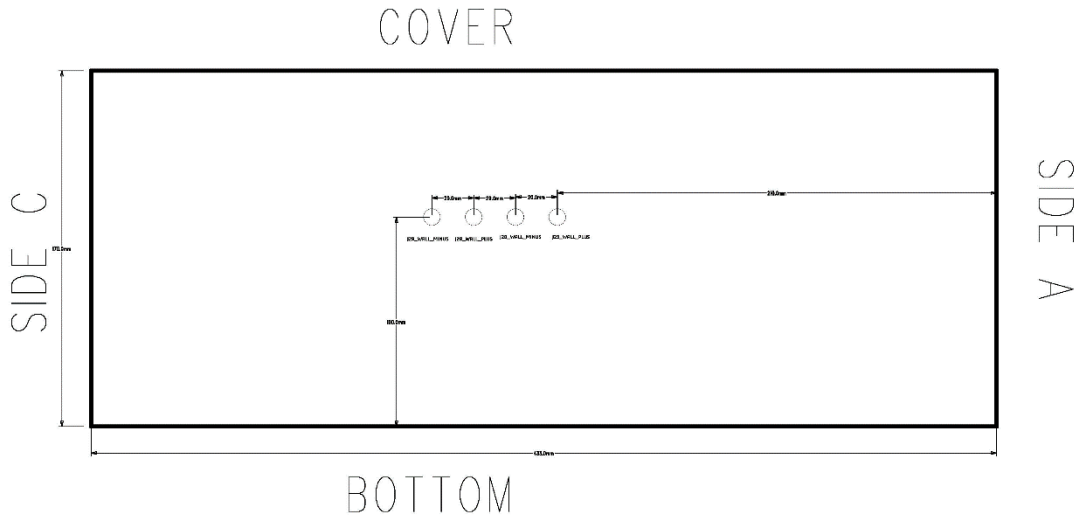


Figure B. 18 Semiconductor Breakout Box Side B Sketch

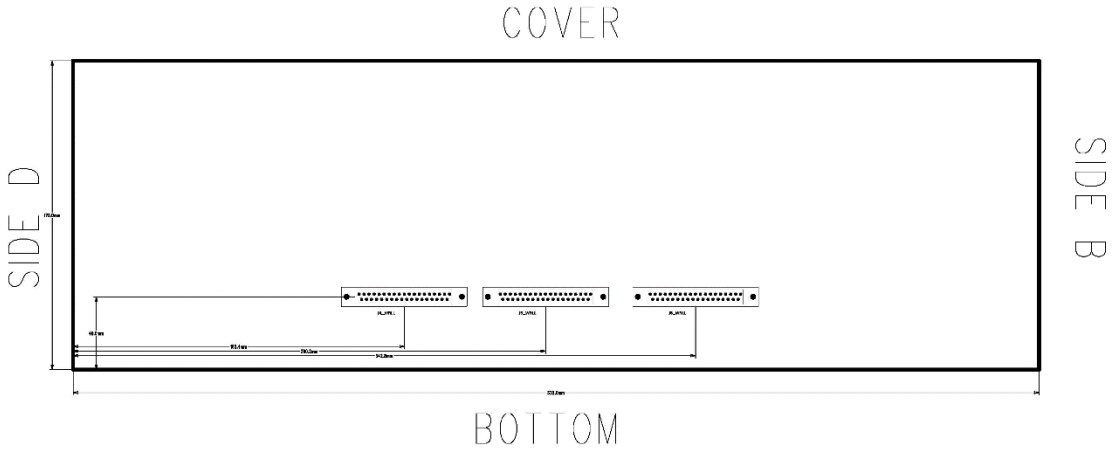


Figure B. 19 Semiconductor Breakout Box Side C Sketch

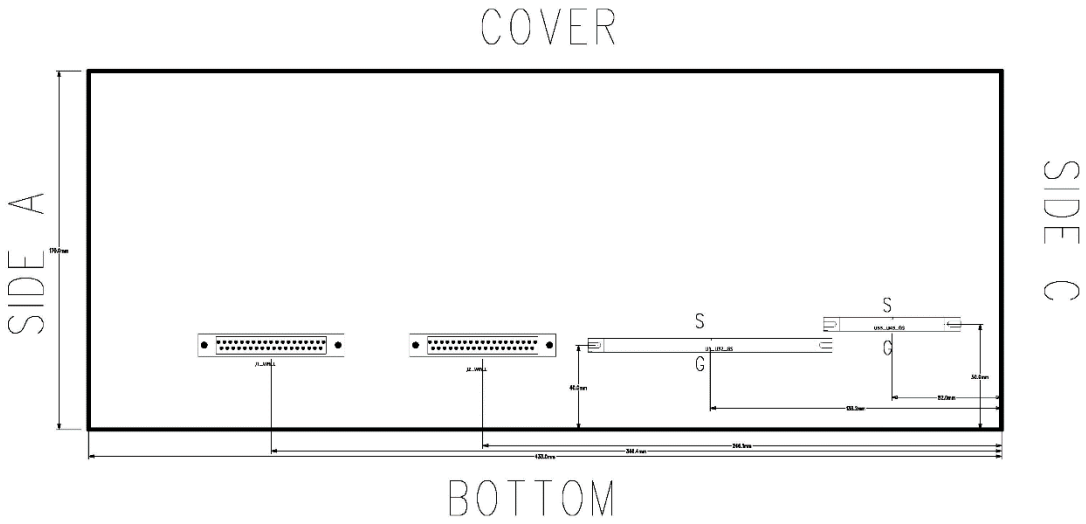


Figure B. 20 Semiconductor Breakout Box Side D Sketch

Table B. 1 Reference designators and descriptions of the components used in Semiconductor Breakout Box

Item	Qty	Ref-Des	Part Name	Desc
1	2	J28-29	1720576	TERM BLOCK HDR 2POS VERT 7.62MM
2	1	J94	74650174R	4 Pin Screw Terminal, Power Tap M4 Through Hole
3	19	D11_D20_AK, D11_D20_RLEAK, D1_D10_AK, D1_D10_RLEAK, U11_U20_GMS, U11_U20_RLEAK, U1_U10_DS, U1_U10_GMS, U1_U10_RLEAK, U21_U20_DS, U21_U30_DS, U21_U30_GMS, U21_U30_RLEAK, U31_U35_DS, U31_U35_GMS, U31_U35_RLEAK, U36_U43_DS, U36_U43_GMS, U36_U43_RLEAK	AWH20G-0222-T	Connector Header Through Hole 20 position 0.100 (2.54mm)"
4	1	U33_U43_GS	AWHW24G-0102-T-R	Connector Header Through Hole 24 position 0.100 (2.54mm)"
5	1	U1_U32_GS	AWHW64G-0202-T	Connector Header Through Hole 64 position 0.100 (2.54mm)"
6	63	R1-63	HRG3216P-1002-B-T1	10 kOhms ±0.1% 1W Chip Resistor 1206 (3216 Metric) Anti-Sulfur, Automotive AEC-Q200, Moisture Resistant Thin Film 24.9 Ohms ±0.01% 0.25W, 1/4W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200 Thin Film 24.9 Ohms ±0.01% 0.25W, 1/4W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200 Thin Film
7	6	J1-6	L77SDCH37SOL2RM8	37 Position D-Sub Receptacle, Female Sockets Connector, Through Hole, Board Lock
8	398	D_ABI1-20, D_ABO1-20, D_KBI1-20, D_KBO1-20, D_RESHM1-15, D_RESHP1-15, D_RESM1-15, D_RESP1-15, U_DBI1-35, U_DBO1-35, U_GB1-43, U_PDBI36-43, U_PDBO36-43, U_PSBI36-43,	SSQ-101-03-T-S	1 Position Receptacle Connector Through Hole Tin

		U_PSBO36-43, U_SB1-43, U_SBI1-35, U_SBO1-35		
SC_BREAKOUTBOX_SURFACE				
Item	**Qty**	**Reference**	**Part Name**	**Desc**
1	338	D_ABI1-20, D_ABO1-20, D_KBI1-20, D_KBO1-20, U_DBI1-35, U_DBO1-35, U_GB1-43, U_PDBI36-43, U_PDBO36-43, U_PSBI36-43, U_PSBO36-43, U_SB1-43, U_SBI1-35, U_SBO1-35	0016020077	Pin Contact Gold 24-30 AWG Crimp
2	43	U_GS1-43	110-73	Toggle Switch SPST Panel Mount
3	19	D11_D20_AK, D11_D20_RLEAK, D1_D10_AK, D1_D10_RLEAK, U11_U20_DS, U11_U20_GMS, U11_U20_RLEAK, U1_U10_DS, U1_U10_GMS, U1_U10_RLEAK, U21_U30_DS, U21_U30_GMS, U21_U30_RLEAK, U31_U35_DS, U31_U35_GMS, U31_U35_RLEAK, U36_U43_DS, U36_U43_GMS, U36_U43_RLEAK	AWH 20G-E202-IDC	20 Position Rectangular Header Connector IDC Gold
4	31	D_RESM1-15, D_RESP1-15, J94	CT2228-0	Banana Jack Connector Standard Banana Solder Black
5	63	D_AK1-20, U_DS1-43	PB1973GBLKGILEF4	Pushbutton Switch DPST Standard, Illuminated Panel Mount, Snap-In
SC_BREAKOUTBOX_SIDE_A				
Item	**Qty**	**Reference**	**Part Name**	**Desc**
1	1	J3_WALL	A-DFF_37LPIII/Z-UNC	37 Position D-Sub Receptacle, Female Sockets Connector
SC_BREAKOUTBOX_SIDE_B				
Item	**Qty**	**Reference**	**Part Name**	**Desc**
1	2	J28_WALL_MINUS,J29_WALL_MINUS	CT2228-0	Banana Jack Connector Standard Banana Solder Black
2	2	J28_WALL_PLUS,J29_WALL_PLUS	CT2228-2	Banana Jack Connector Standard Banana Solder Red
SC_BREAKOUTBOX_SIDE_C				
Item	**Qty**	**Reference**	**Part Name**	**Desc**
1	3	J4_WALL,J5_WALL,J6_WALL	A-DFF 37LPIII/Z-UNC	37 Position D-Sub Receptacle, Female Sockets Connector
SC_BREAKOUTBOX_SIDE_D				
Item	**Qty**	**Reference**	**Part Name**	**Desc**
1	2	J1_WALL,J2_WALL	A-DFF_37LPIII/Z-UNC	37 Position D-Sub Receptacle, Female Sockets Connector
2	1	U33_U43_GS	AWH-24G-E202-IDC	24 Position Rectangular Header Connector IDC Gold
3	1	U1_U32_GS	AWH-64G-E202-IDC	64 Position Rectangular Header Connector IDC Gold

APPENDIX C: MOSFET GATE CONTROL BOARD SIMULATIONS

Used component simulation models were either from PSpice libraries, or downloaded from the web pages of the manufactures. Capacitor simulation models were downloaded from Würth Elektronik. The simulations are used as a reference in designing MOSFET Gate Control Board. Supply and reference voltages were not necessarily applicable to the built prototype.

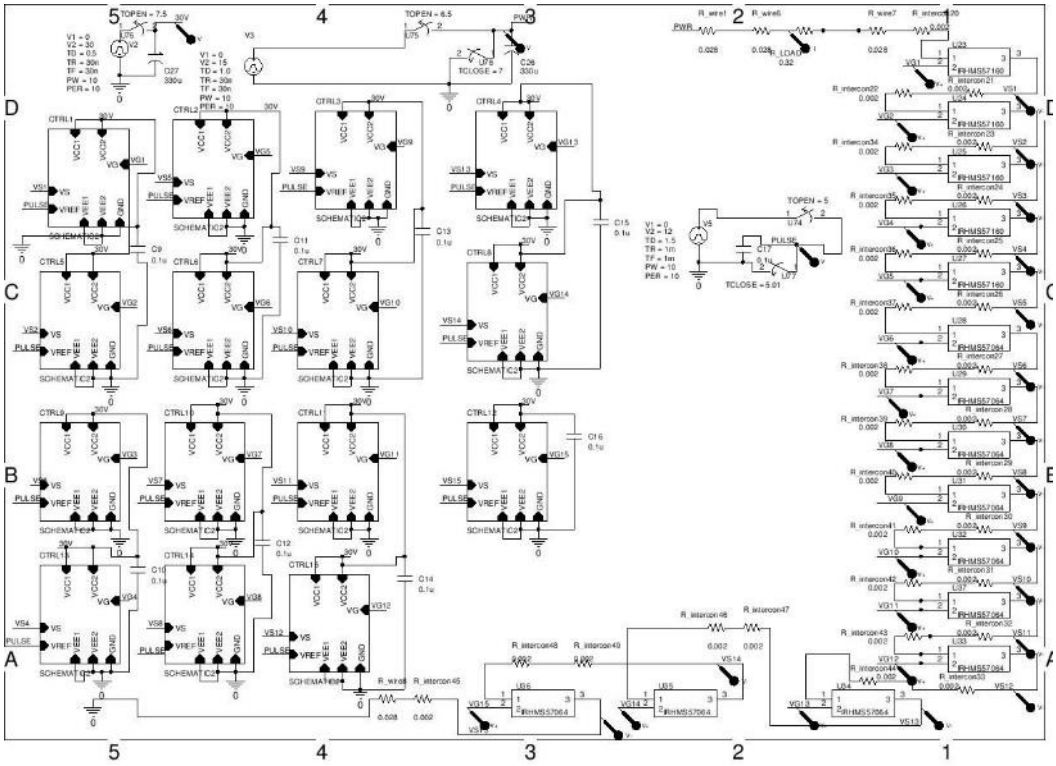


Figure C. 1 25 A series connection circuit used in PSpice Simulations.

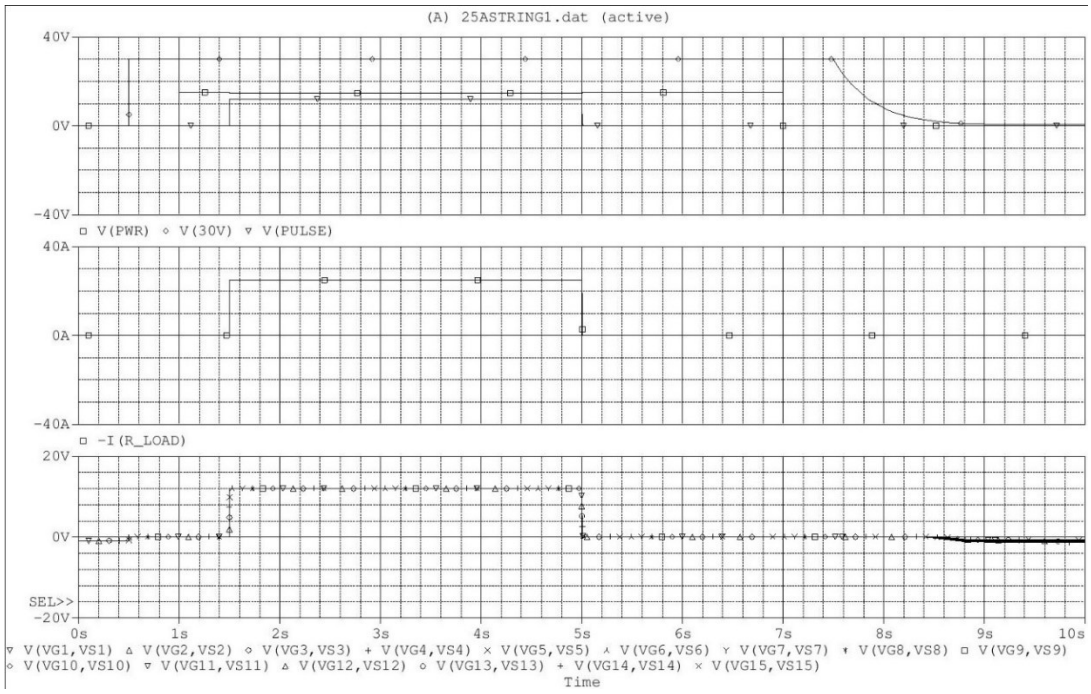


Figure C. 2 25 A connection Transient Simulation Results. Due to SCTW100N65G2AG simulation model unavailability, it was replaced by IRHMS57064 in the simulations. The details of CTRL circuits in the Schematic are in Figure 5.10

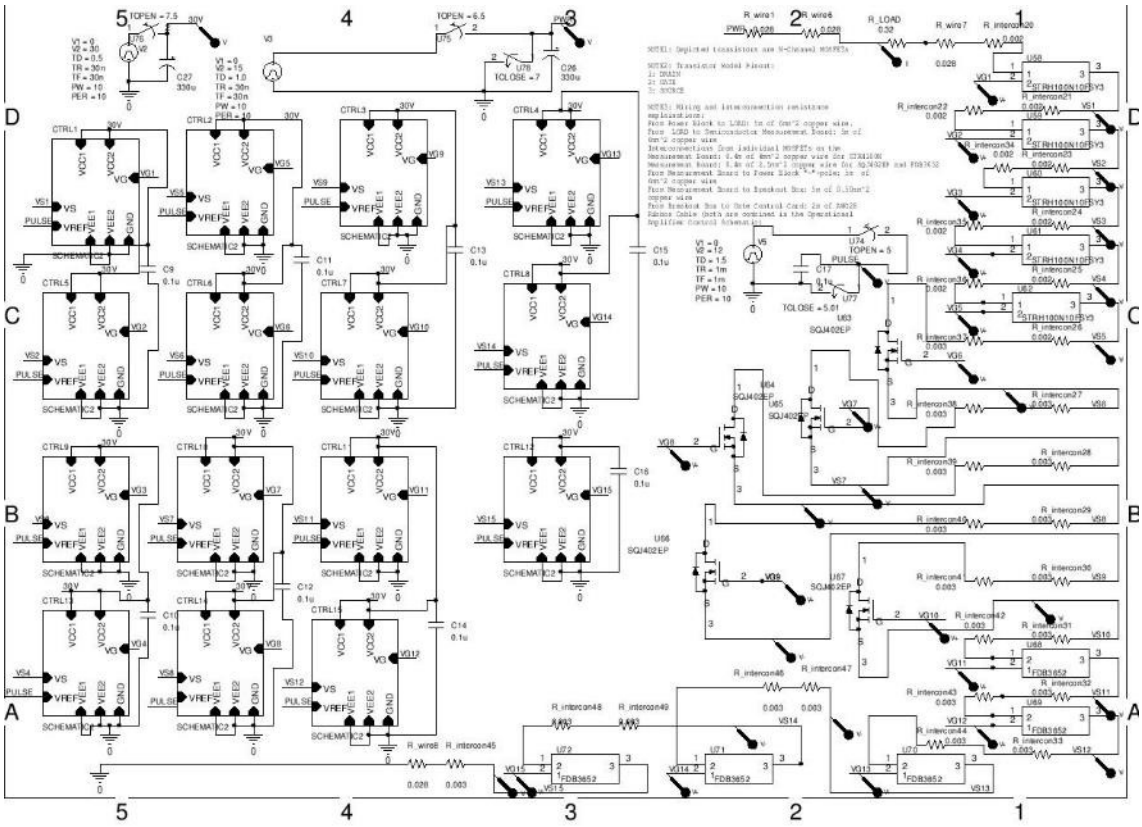


Figure C. 3 20 A series connection circuit used in PSpice Simulations. The details of CTRL circuits in the Schematic are in Figure 5.10

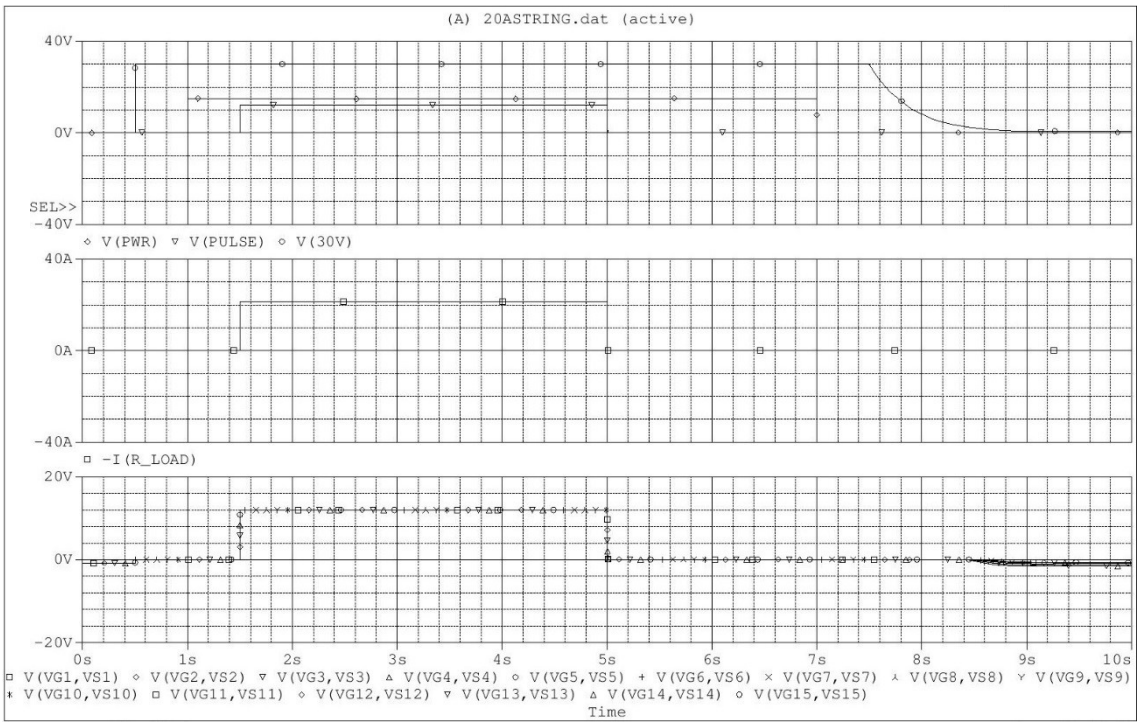


Figure C. 4 20 A series connection Transient Simulation Results

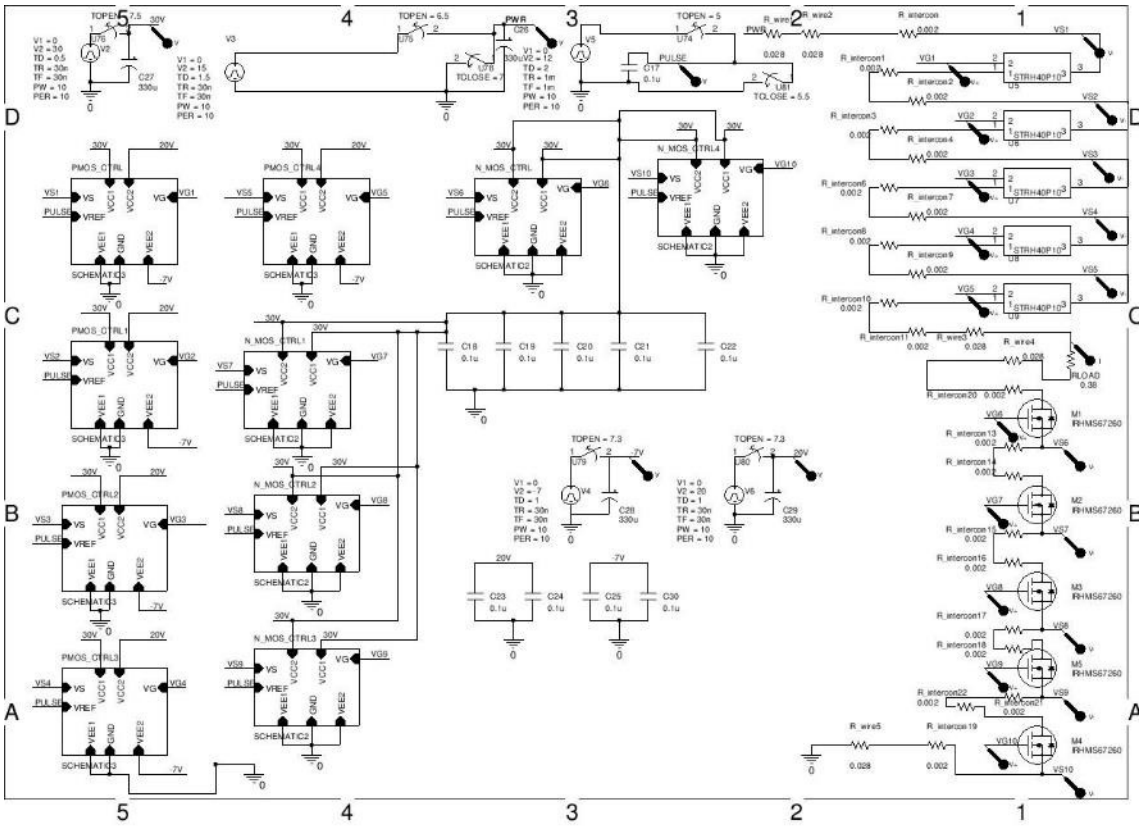


Figure C. 5 15 A series connection circuit used in PSpice Simulations. The details of NMOS_CTRL circuits in the Schematic are in Figure 5.10. The details of PMOS_CTRL circuits in the Schematic are in Figure 5.11

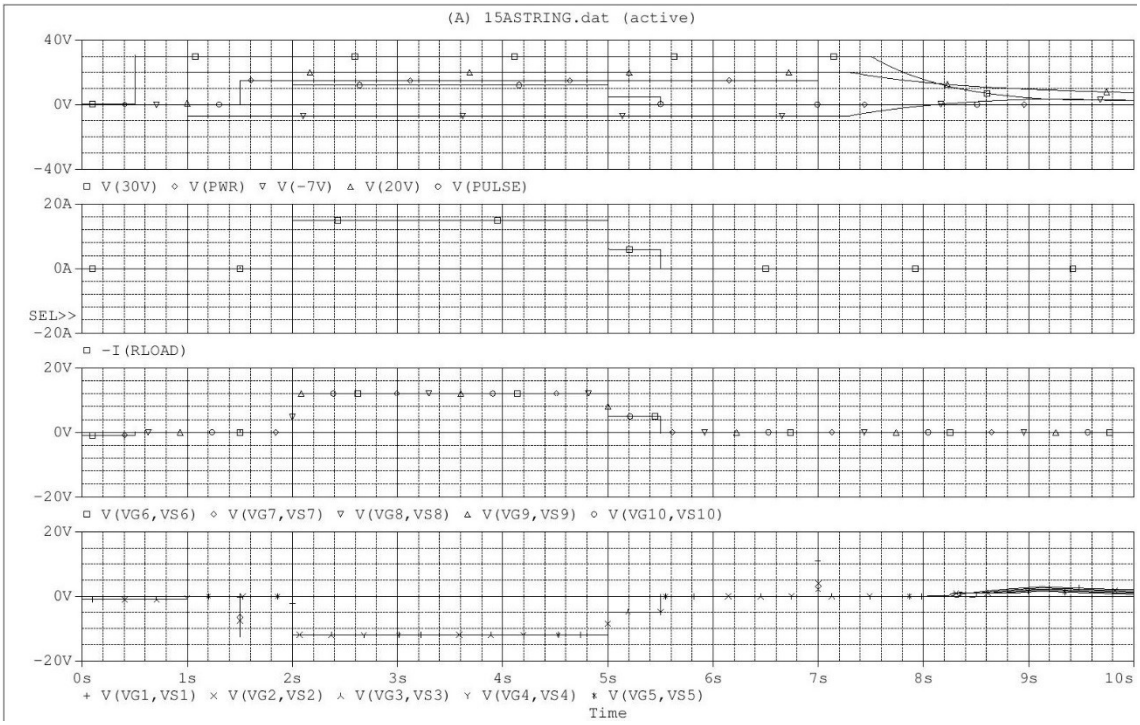


Figure C. 6 15 A series connection Transient Simulation Results

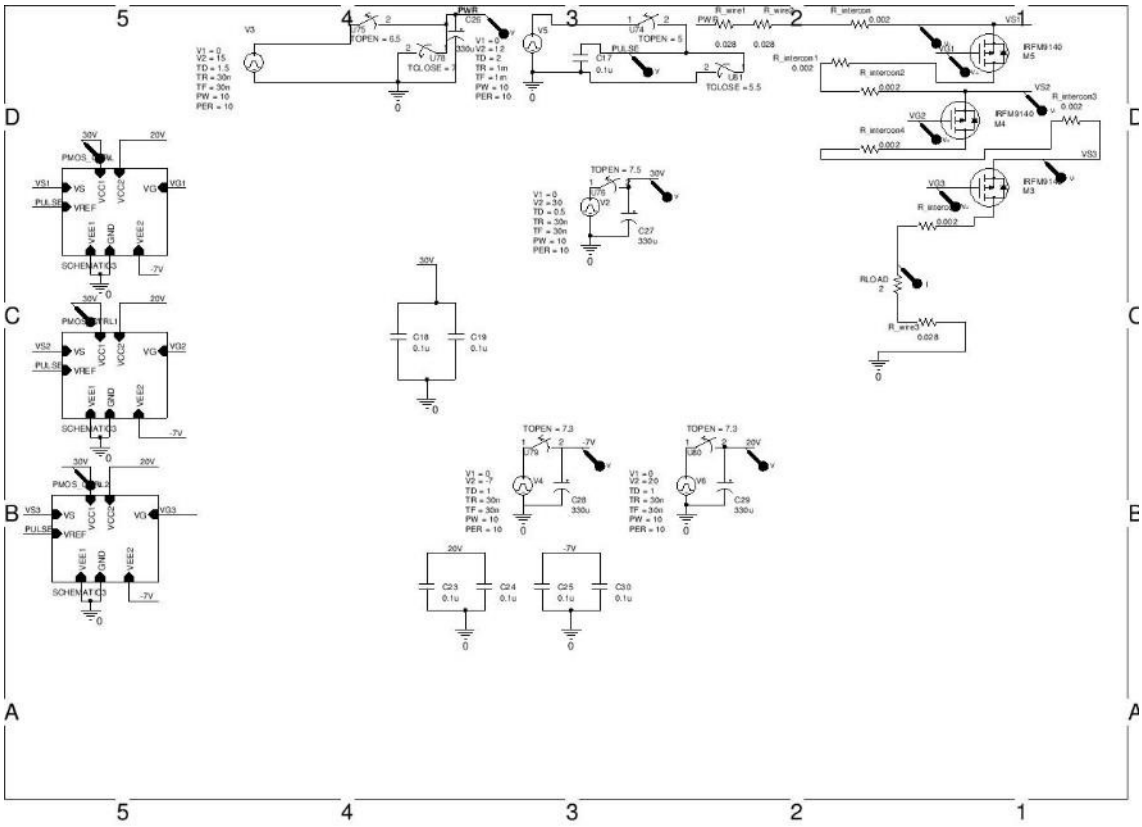


Figure C. 7 6 A series connection circuit used in PSpice Simulations. The details of PMOS_CTRL circuits in the Schematic are in Figure 5.11

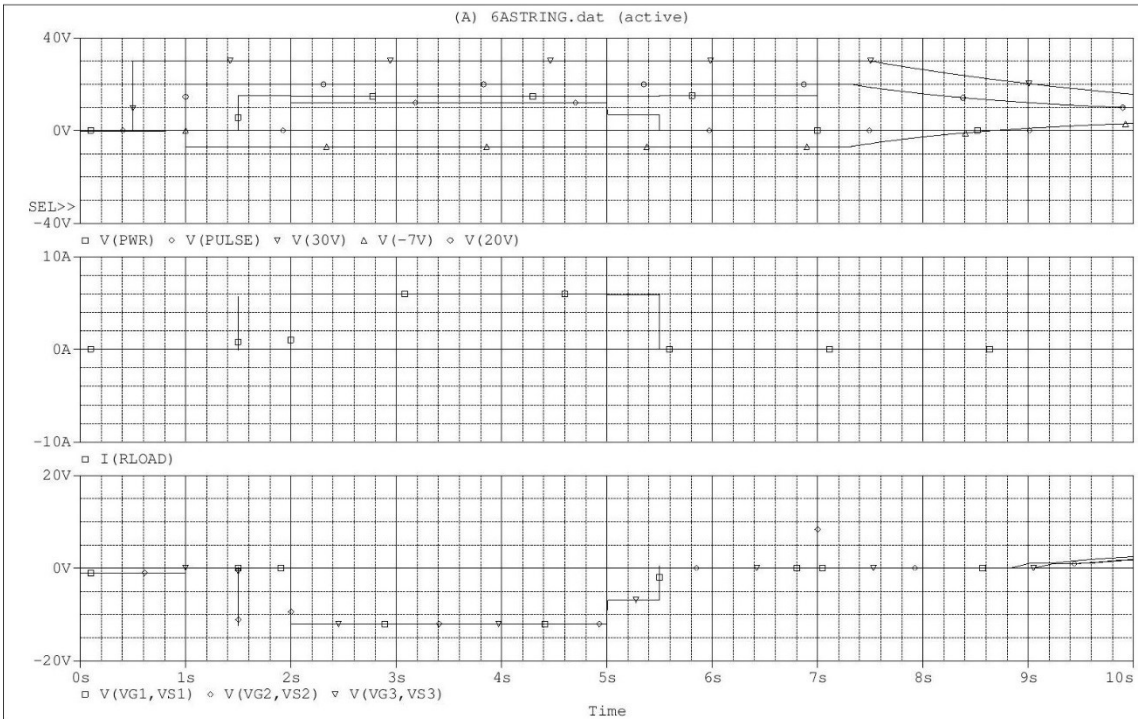


Figure C. 8 6 A series connection Transient Simulation Results. In case of only p-channel MOSFET connections the transistors turn briefly when the power supply used to provide current for the series connection is either turned on or off (1.5 s and 7 s)

APPENDIX D: MOSFET GATE CONTROL BOARD

Due to the several mistakes made in the design of this board (KA7909 and protection Zener diode wiring in particular) the schematic and layout need to be redesigned.

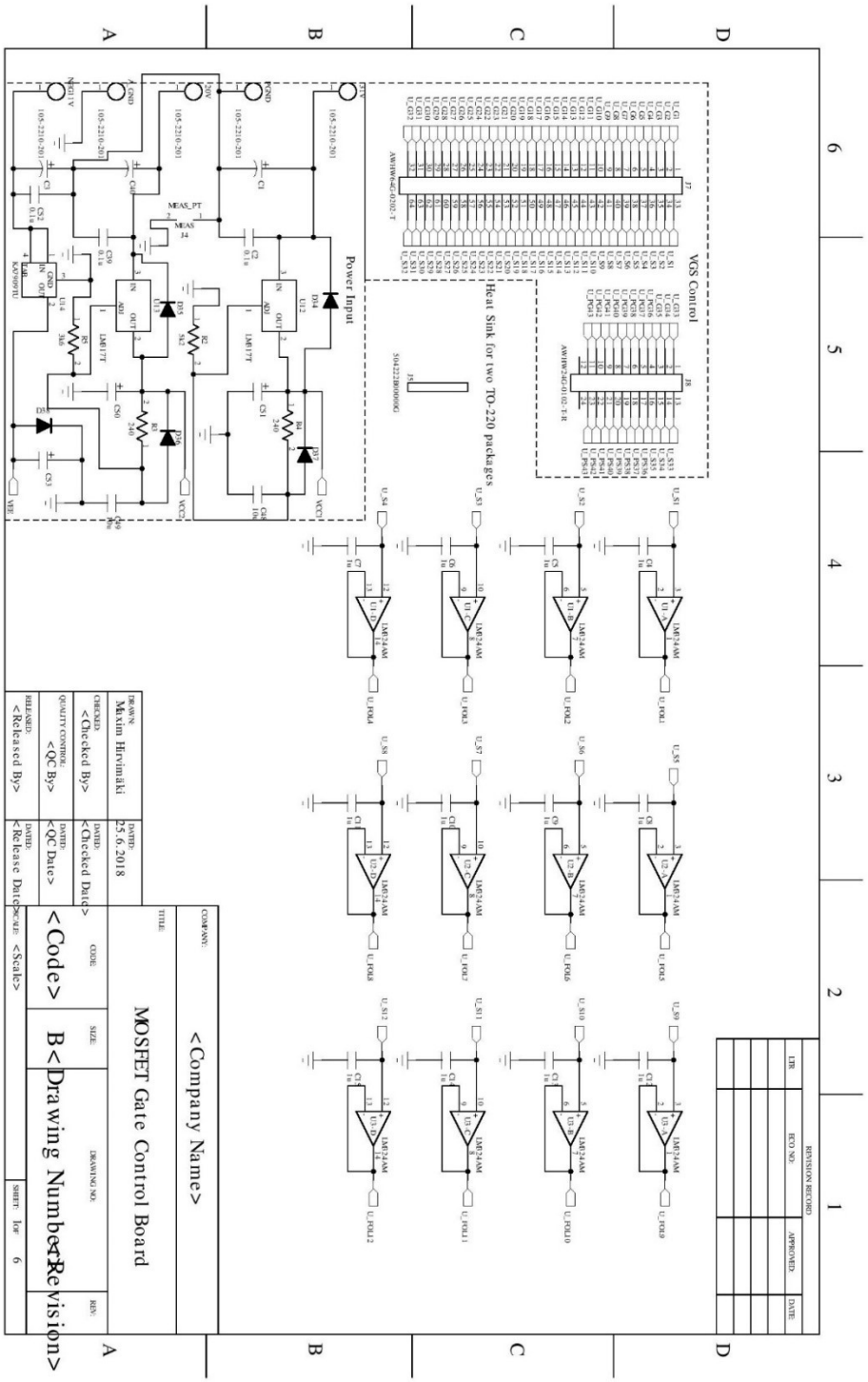


Figure D. 1 MOSFET Gate Control Board Schematic page 1

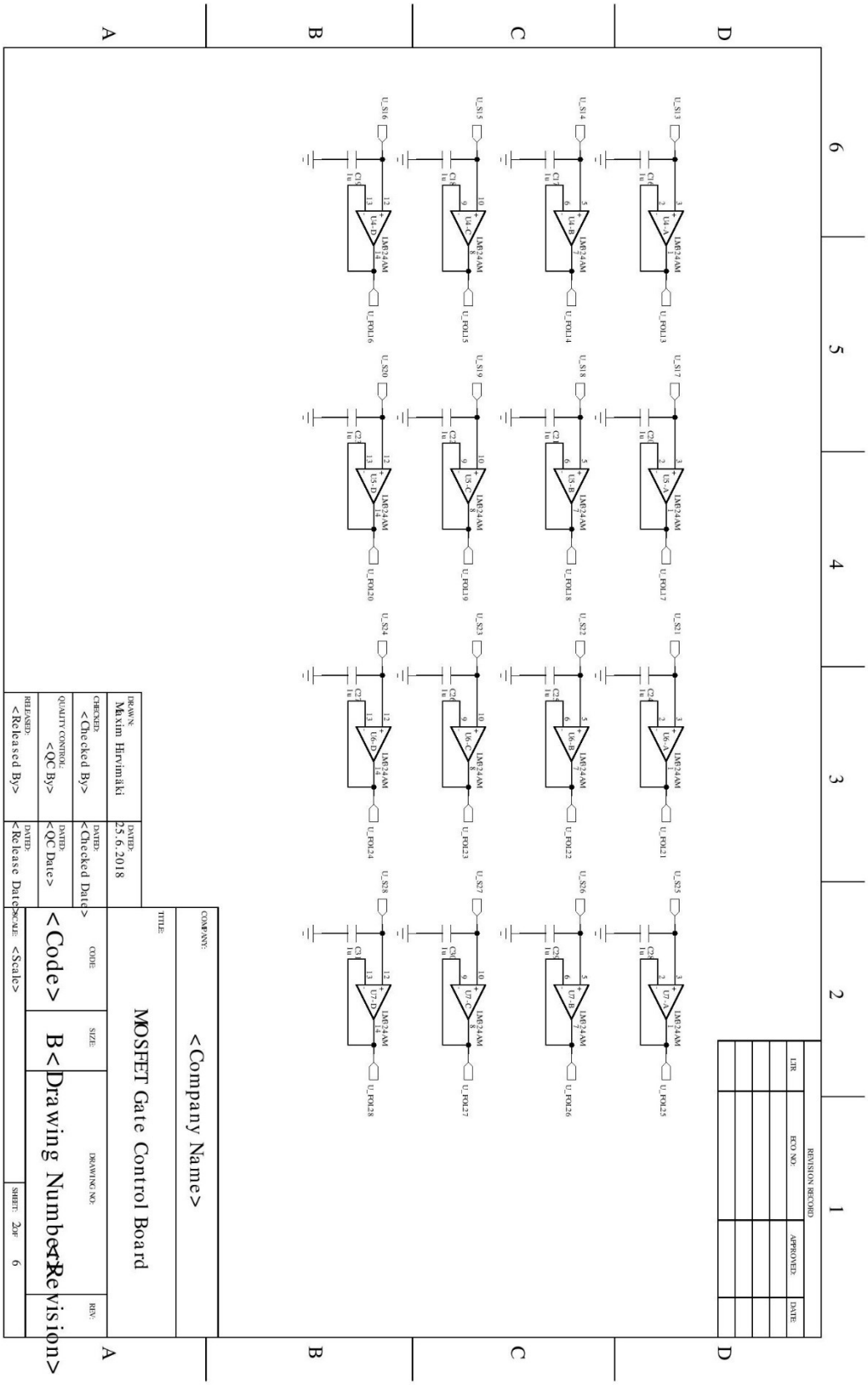


Figure D. 2 MOSFET Gate Control Board Schematic page 2

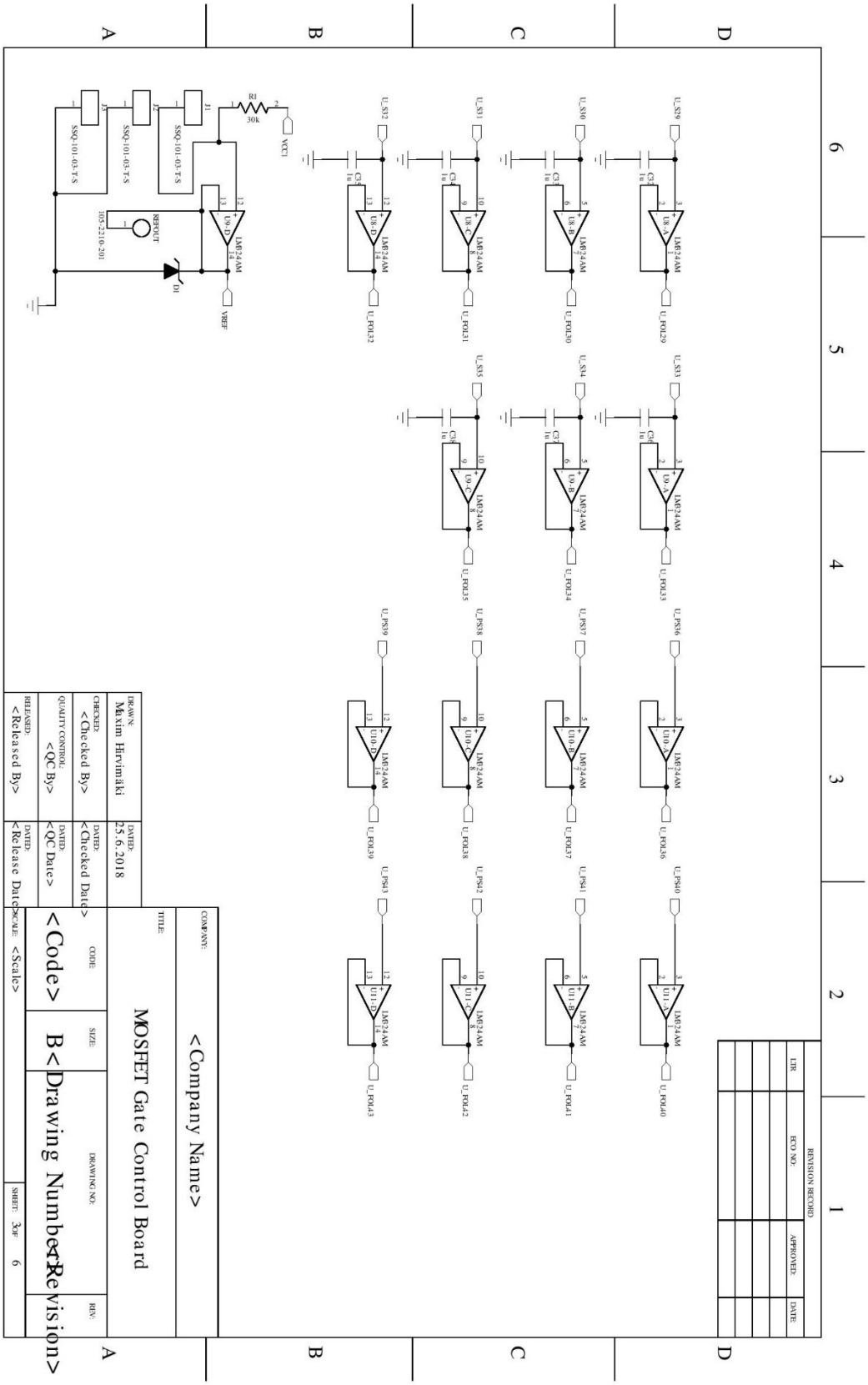


Figure D. 3 MOSFET Gate Control Board Schematic page 3

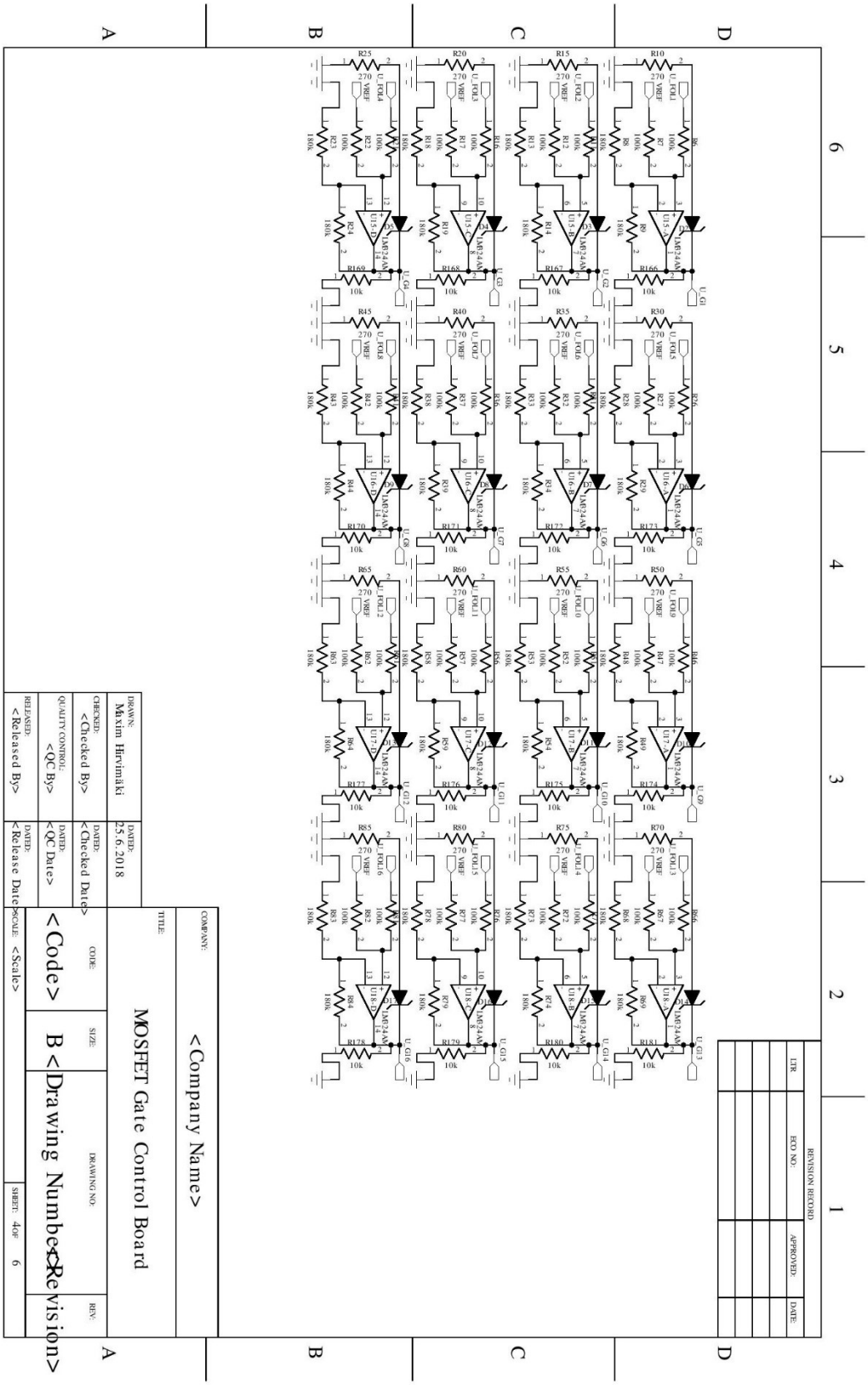


Figure D. 4 MOSFET Gate Control Board Schematic page 4

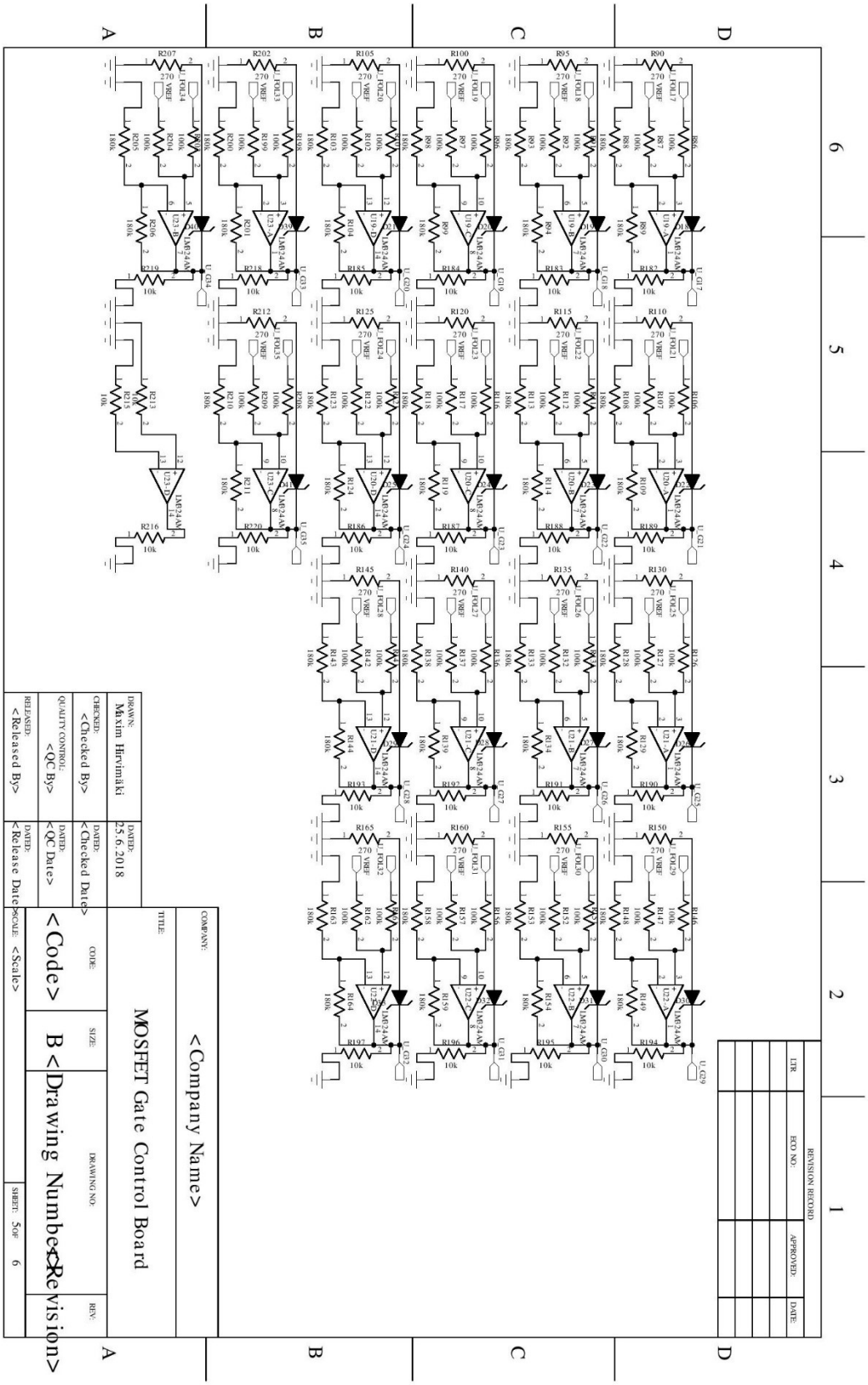


Figure D. 5 MOSFET Gate Control Board Schematic page 5

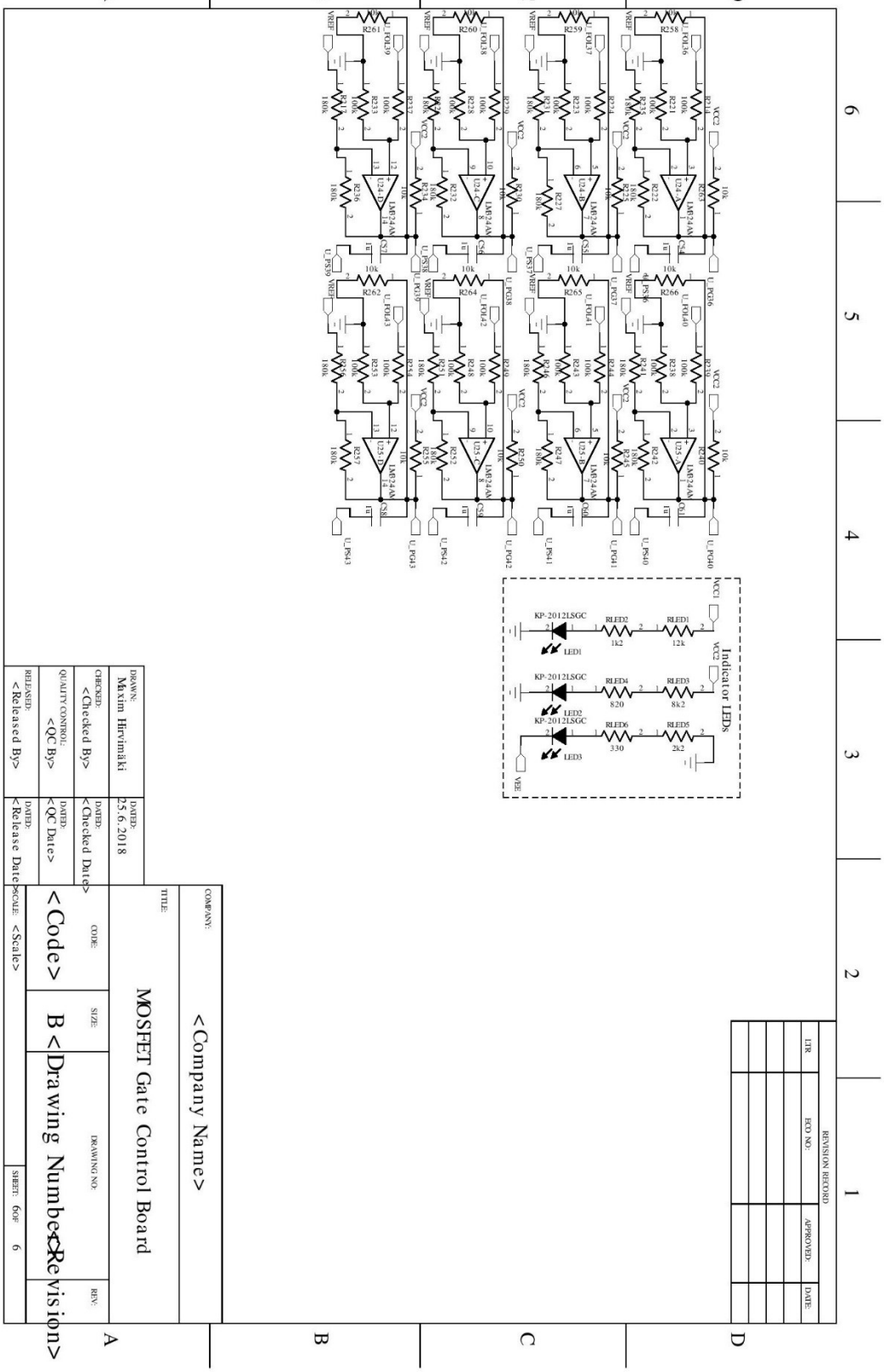


Figure D. 6 MOSFET Gate Control Board Schematic page 6

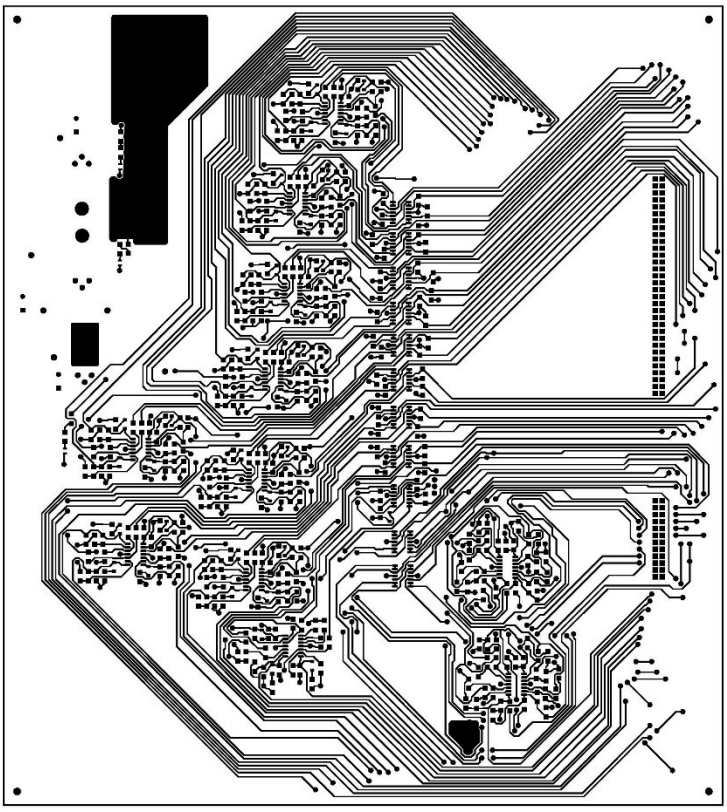


Figure D. 7 MOSFET Gate Control Board PCB Mask Top

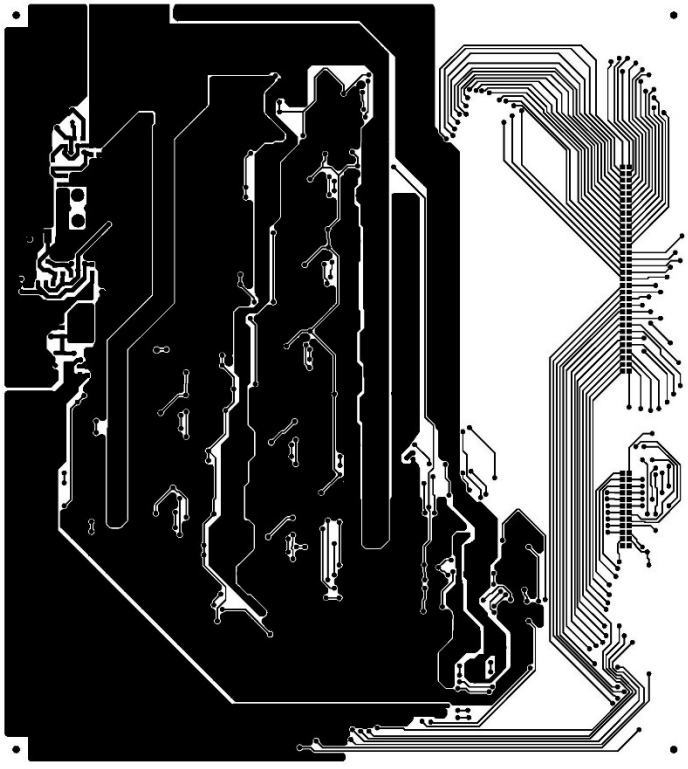


Figure D. 8 MOSFET Gate Control Board PCB Mask Bottom

Figure D. 9 MOSFET Gate Control Board Assembly diagram Top (with vias included). PCB size 300 mm x 265 mm.

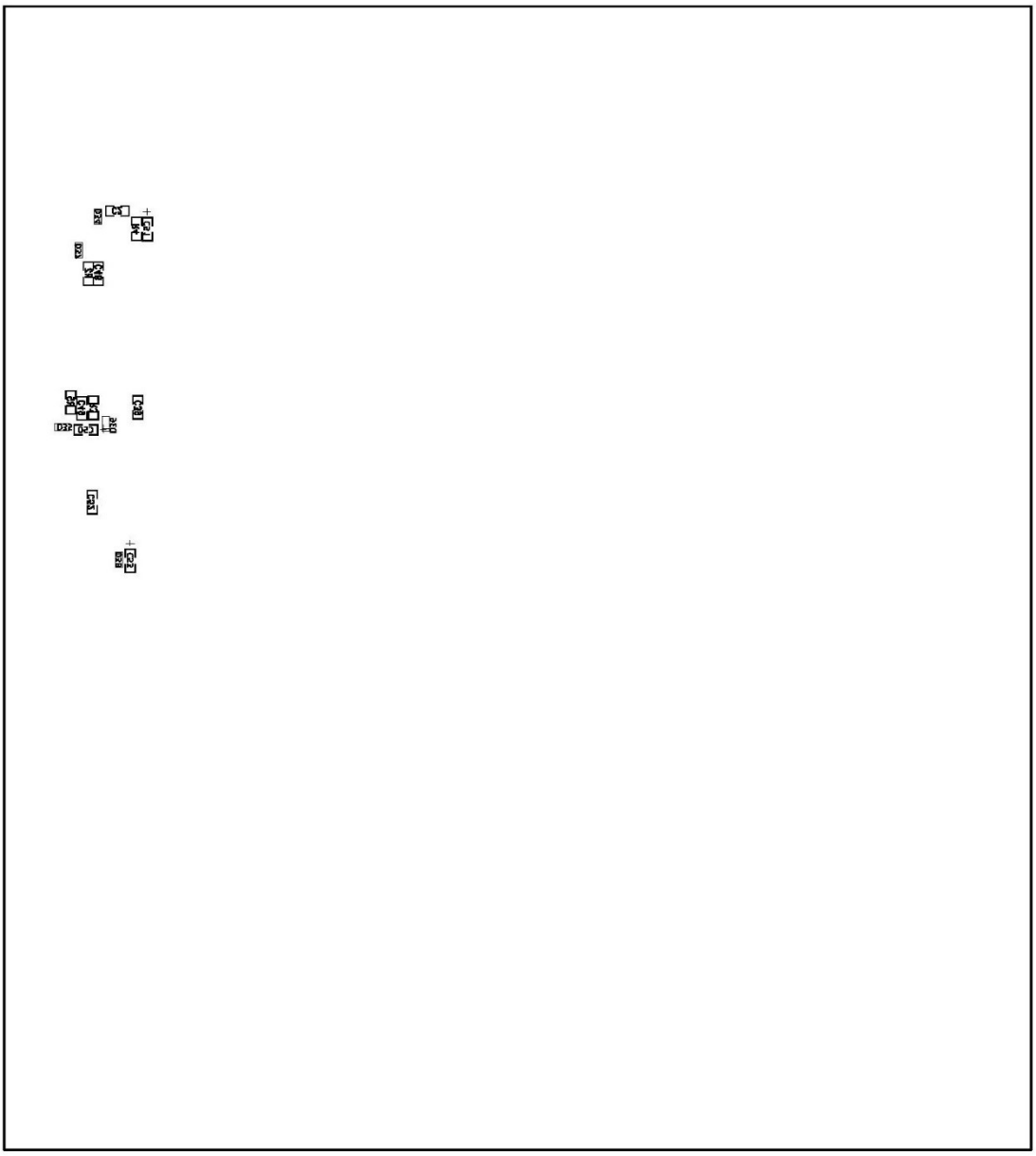
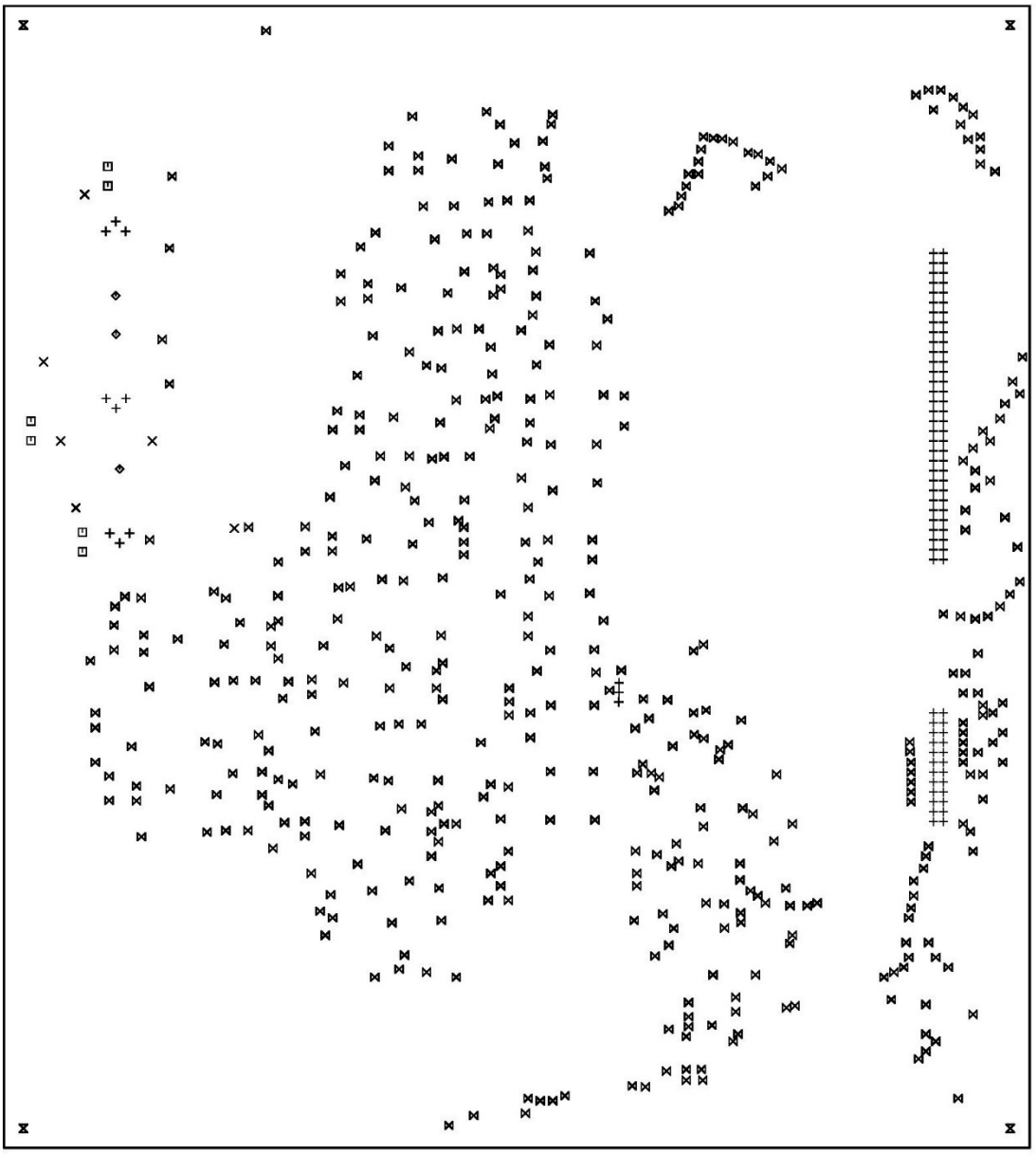


Figure D. 10 MOSFET Gate Control Board diagram Bottom



SIZE	QTY	SYM	PLATED	TOL
1.02	100	+	YES	+/-0.0
1.32	6	X	YES	+/-0.0
0.9	6	□	YES	+/-0.0
3.81	3	◇	YES	+/-0.0
5	4	⧖	YES	+/-0.0
1	449	⋈	YES	+/-0.0

Figure D. 11 MOSFET Gate Control Board Drill diagram

Table D. 1 Reference designators and descriptions of the components used in MOSFET Gate Control Board

Item	Qty	Ref-Des	Part Name	Desc
1	1	U14	KA799TU	Linear Voltage Regulator, 7909, Fixed, -35V To -10V In, -9V And 1A Out, TO-220AB-3
2	2	U12-13	LM317T	POSITIVE VOLTAGE REGULATOR; ADJUSTABLE
3	22	U1-11,U15-25	LM324	QUAD,LOW POWER OP AMP
4	1	R1	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 240, 1/8W
5	1	R4	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 240, 1/8W
6	19	R90,R95,R100,R105,R110,R115,R120,R125,R130,R135,R140,R145,R150,R155,R160,R165,R202,R207,R212	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 270, 1/8W
7	6	20V,31V,A_GND,NEG11V,PGND,REFOUT	105-2210-201	Tip Jack Connector Standard Tip Solder Blue
8	43	C4-38,C54-61	1206 Ceramic Capacitor	Surface Mount Ceramic Capacitor, 1206 [3216 Metric], 1u,50V
9	2	C48-49	1206 Ceramic Capacitor	Surface Mount Ceramic Capacitor, 1206 [3216 Metric], 10u,50V
10	1	R2	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 5.2k, 1/8W
11	1	R3	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 240, 1/8W
12	1	R5	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 3.6k, 1/8W
13	86	R6-7,R11-12,R16-17,R21-22,R26-27,R31-32,R36-37,R41-42,R46-47,R51-52,R56-57,R61-62,R66-67,R71-72,R76-77,R81-82,R86-87,R91-92,R96-97,R101-102,R106-107,R111-112,R116-117,R121-122,R126-127,R131-132,R136-137,R141-142,R146-147,R151-152,R156-157,R161-162,R198-199,R203-204,R208-209,R214,R221,R223-224,R228-229,R233,R237-239,R243-244,R248-249,R253-254	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 100k, 1/8W
14	70	R93-94,R9,R43,R98-99,R44,R103-104,R13,R23,R108-109,R48-49,R113-114,R24,R118-119,R53,R123-124,R54,R128-129,R14,R133-134,R58-59,R138-139,R28,R143-144,R29,R63,R148-149,R64,R153-154,R158-159,R68-69,R163-164,R8,R200-201,R33,R73,R205-206,R74,R210-211,R34,R78-79,R18-19,R83-84,R38-39,R88-89	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 180k, 1/8W
15	54	R178-197,R166,R213,R167,R215-216,R218-220,R168-169,R225,R170,R230,R171,R234,R172-173,R240,R174-	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 10k, 1/8W

		175,R245,R176-177,R250,R255,R258-266		
16	16	R235-236,R217,R241-242,R246-247,R222,R251-252,R256-257,R226-227,R231-232	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric],180k, 1/8W
17	16	R45,R25,R40,R20,R50,R35,R60,R55,R85,R80,R70,R15,R65,R75,R30,R10	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 270, 1/8W
18	1	RLED1	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 12k, 1/8W
19	1	RLED2	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 1.2k, 1/8W
20	1	RLED3	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 8.2k, 1/8W
21	1	RLED4	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 820, 1/8W
22	1	RLED5	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 2.2k, 1/8W
23	1	RLED6	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 330, 1/8W
24	1	C53	1206 Tantalum Capacitor	Surface Mount Tantalum Capacitor, 1206 [3216 Metric],1u,50V
25	1	C50	1206 Tantalum Capacitor	Surface Mount Tantalum Capacitor, 1206 [3216 Metric], 1u, 50V
26	1	C51	1206 Tantalum Capacitor	Surface Mount Tantalum Capacitor, 1206 [3216 Metric], 1u, 50V
27	1	J5	504222B00000G	Heat Sink, Square, PCB, 6.4 °C/W, TO-220, 19.81 mm, 21.59 mm, 36.83 mm
28	1	C40	Electrolytic Capacitor, 100u, 50V	100µF 50V Aluminum Electrolytic Capacitors Radial, Can
29	1	J7	AWHW 64G-0202-T	Connector Header Through Hole 64 position 0.100 (2.54mm)"
30	1	J8	AWHW24G-0102-T-R AWHW24G-0102-T-R	Connector Header Through Hole 24 position 0.100 (2.54mm)"
31	3	C2,C39,C52	Ceramic Capacitor 1206	Surface Mount Ceramic Capacitor, 1206 [3216 Metric], 0.1u,50V
32	1	C3	Electrolytic Capacitor, 100u, 50V	100µF 50V Aluminum Electrolytic Capacitors Radial, Can
33	1	C1	Electrolytic Capacitor, 330u, 50V	330µF 50V Aluminum Electrolytic Capacitors Radial, Can
NON PCB				
50k Potentionmeter for VREF				Connected to J1, J2, J3

APPENDIX E: MINIATURE SEMICONDUCTOR MEASUREMENT BOARD

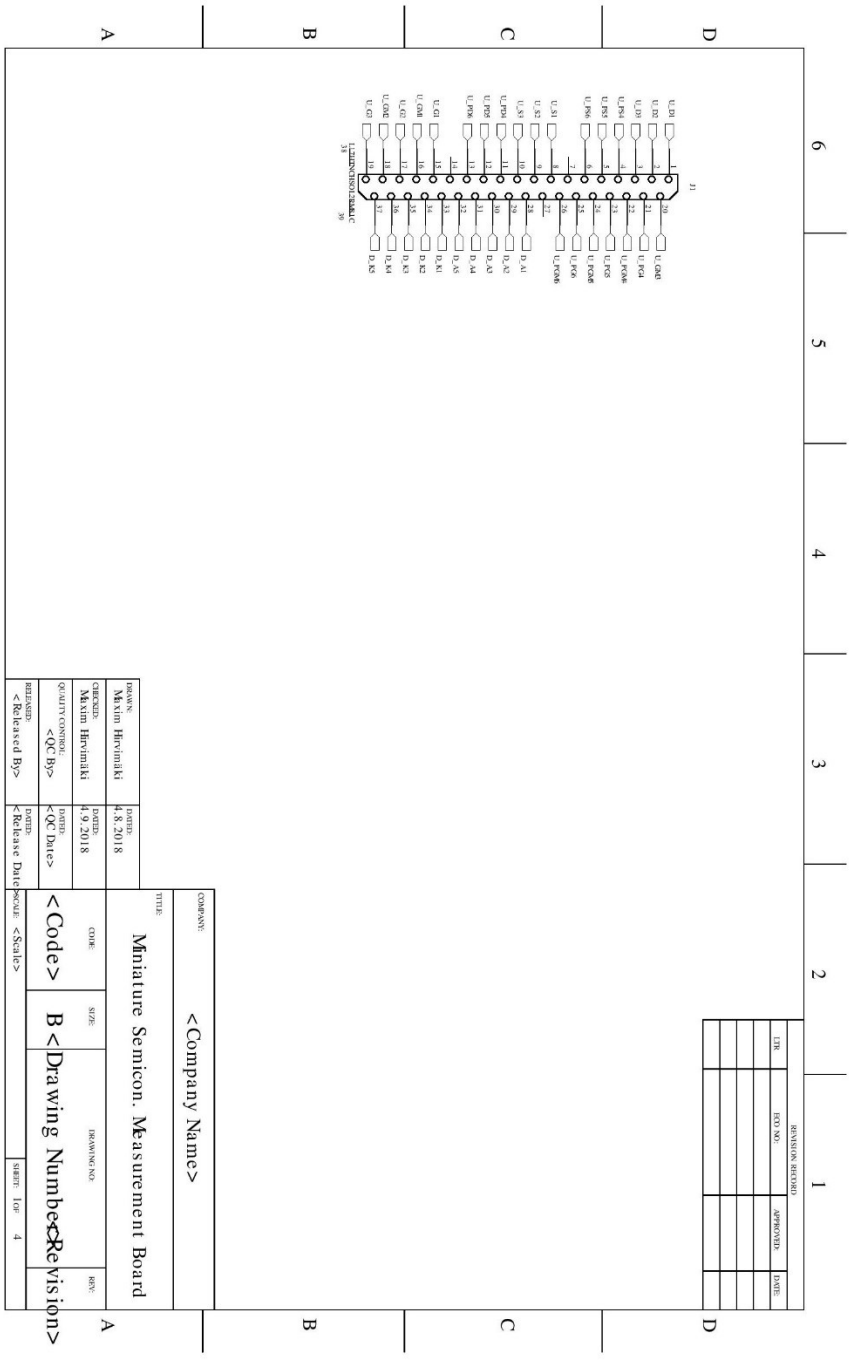


Figure E. 1 Miniature Semiconductor Measurement Board Schematic page 1

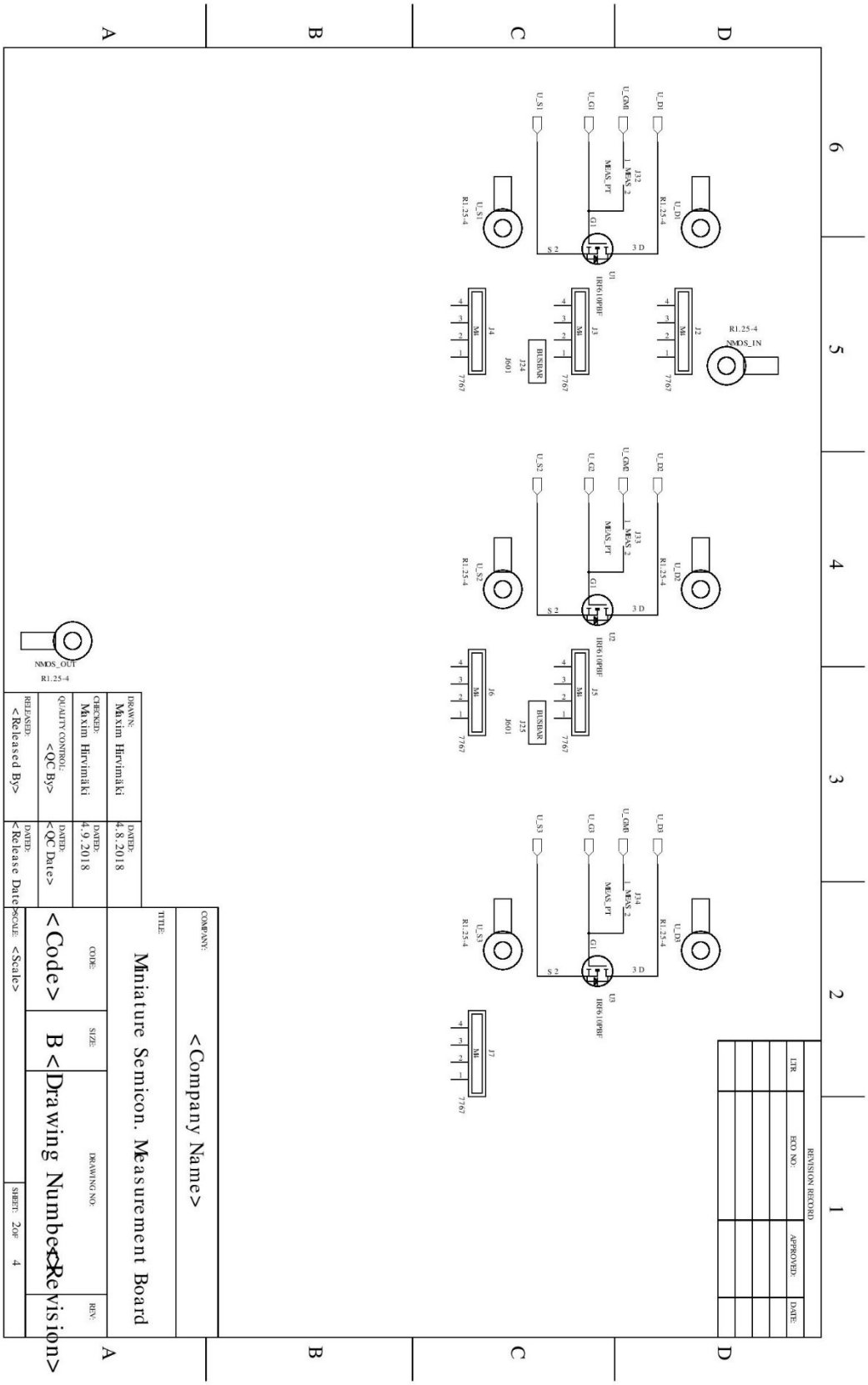


Figure E. 2 Miniature Semiconductor Measurement Board Schematic page 2

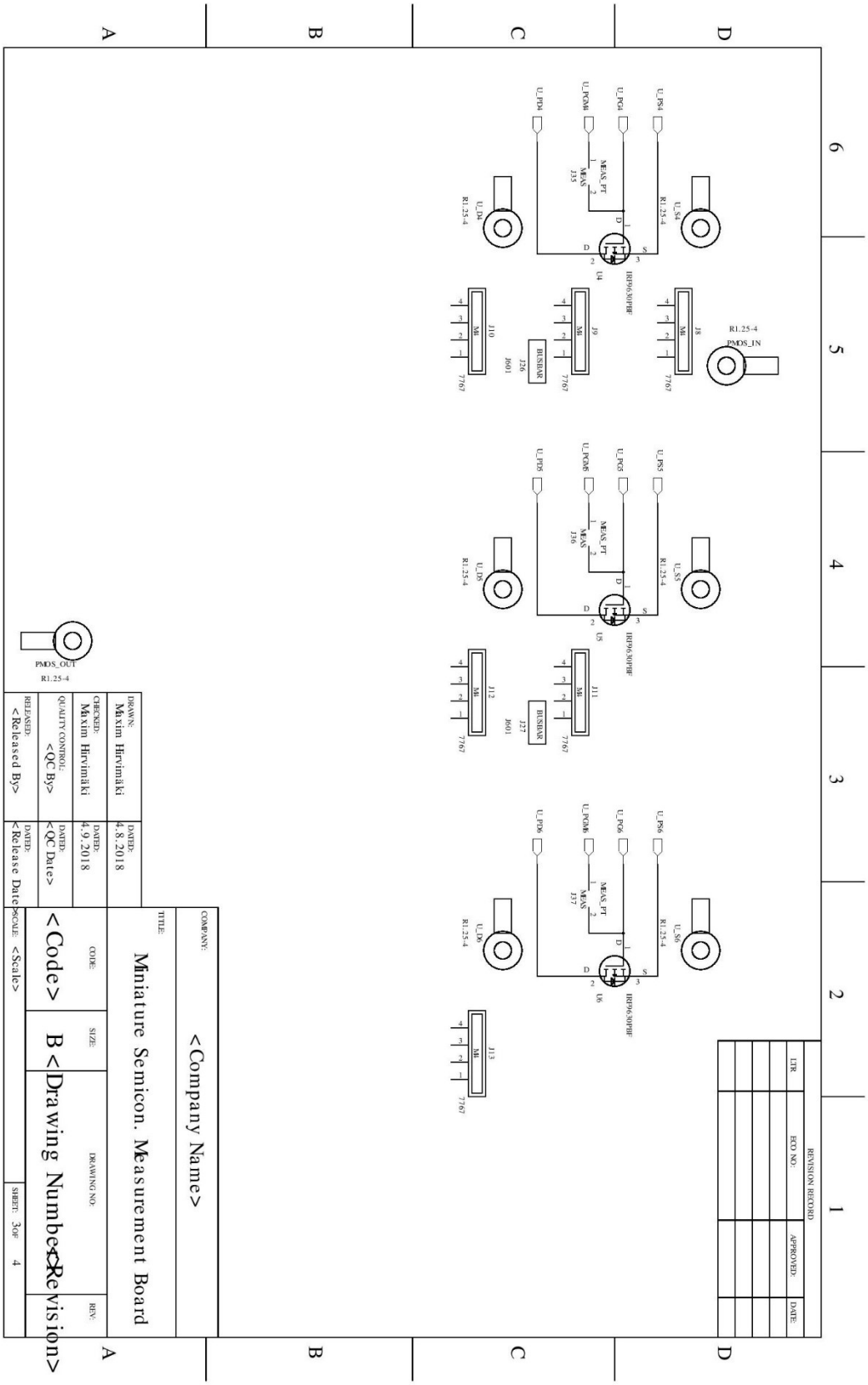


Figure E. 3 Miniature Semiconductor Measurement Board Schematic page 3

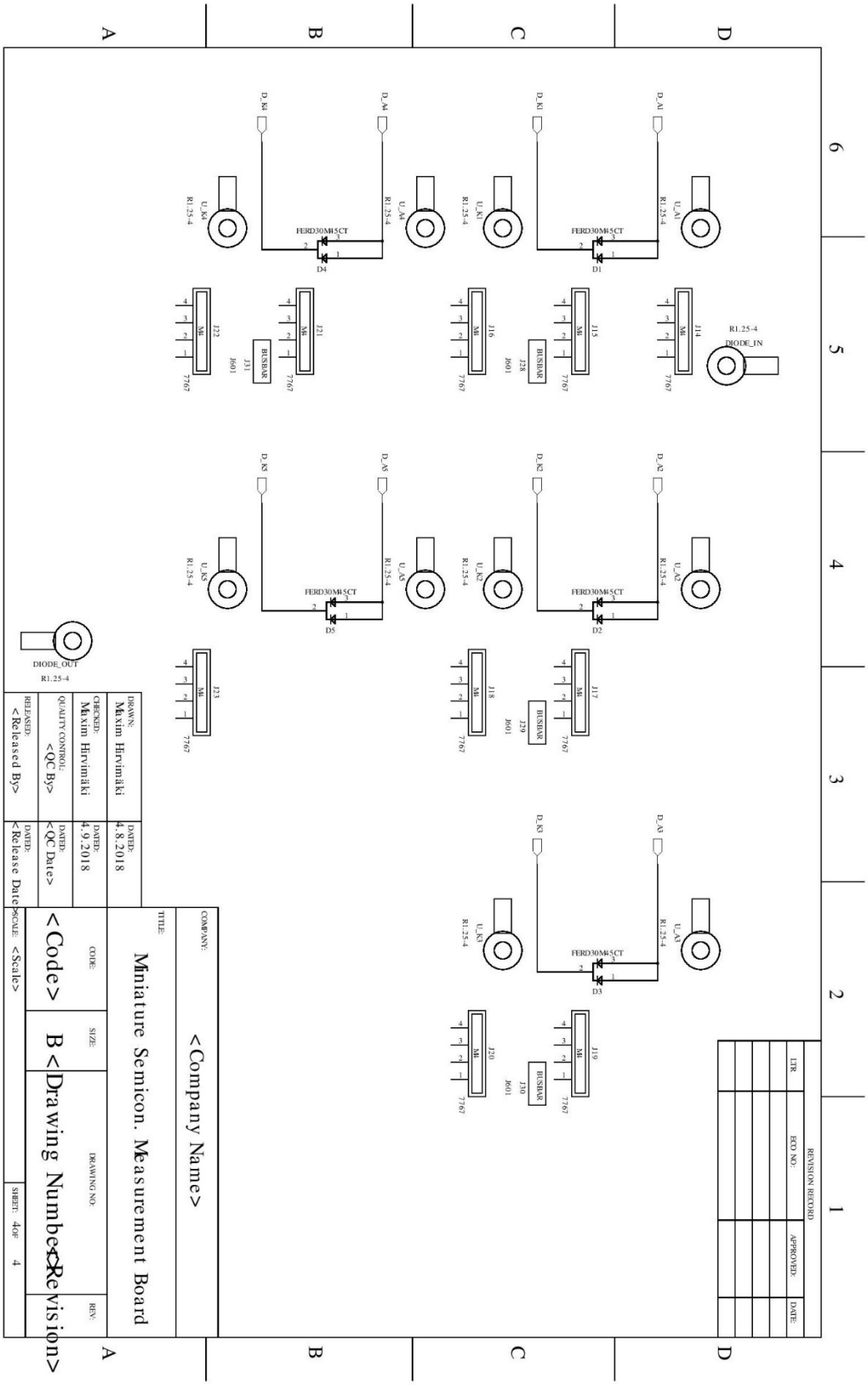


Figure E. 4 Miniature Semiconductor Measurement Board Schematic page 4

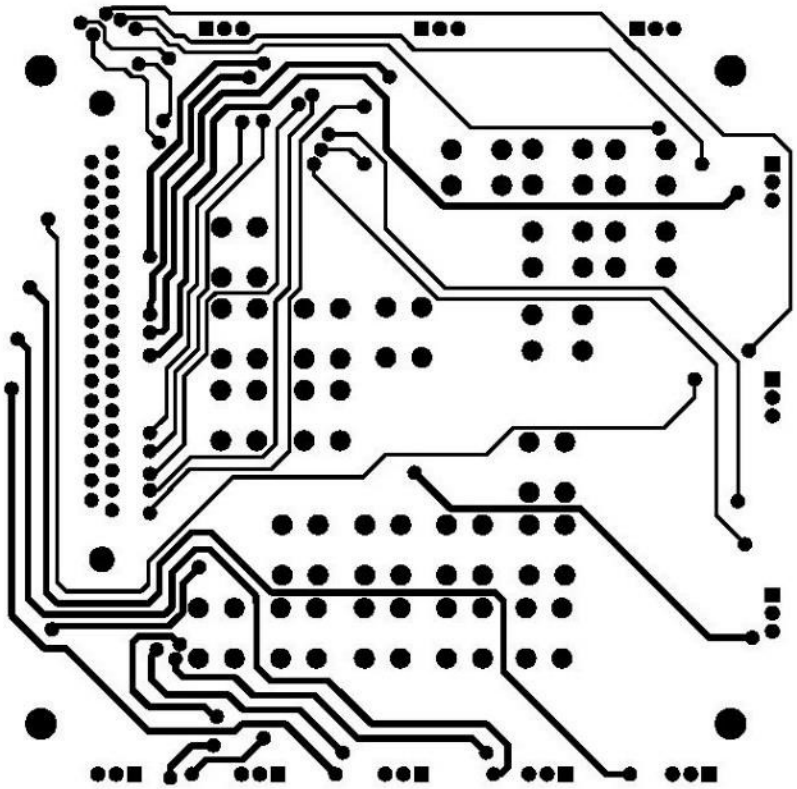


Figure E. 5 Miniature Semiconductor Measurement Board PCB Mask Top

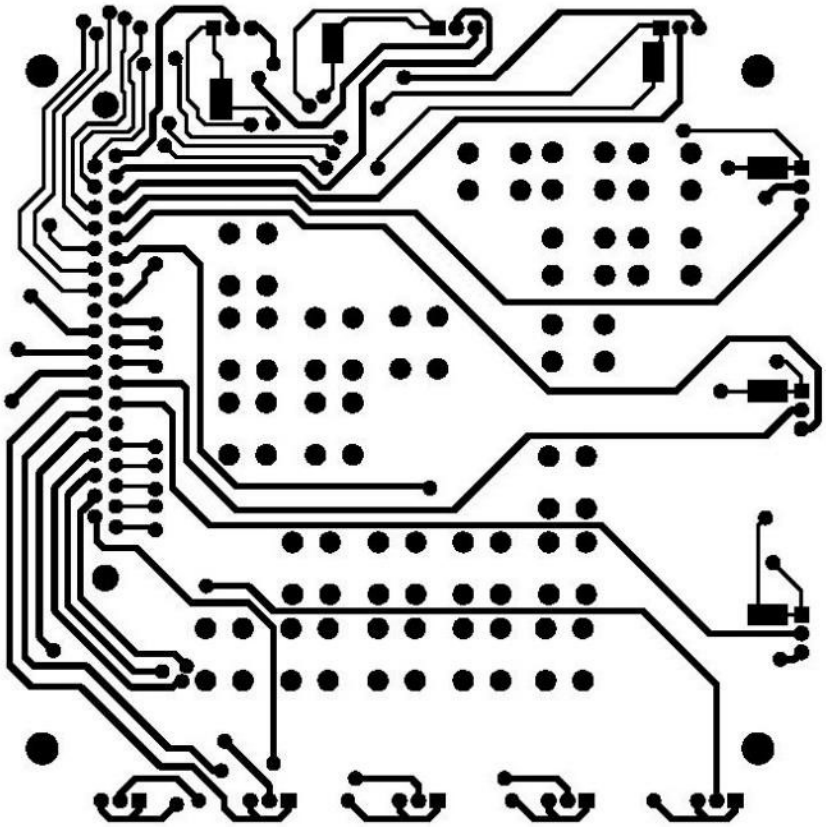


Figure E. 6 Miniature Semiconductor Measurement Board PCB Mask Bottom

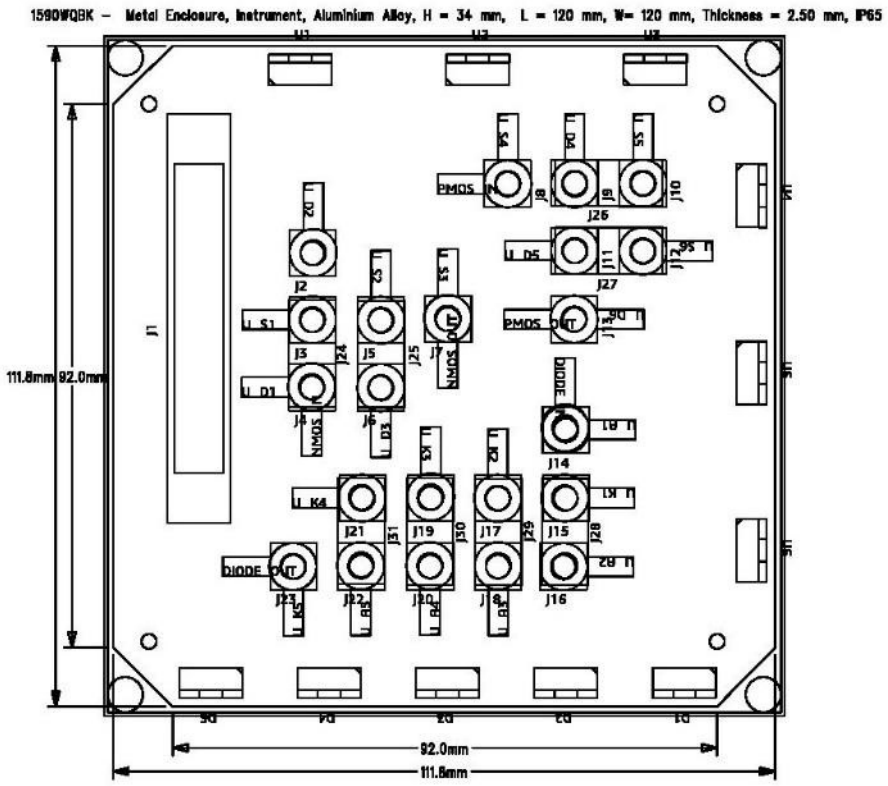
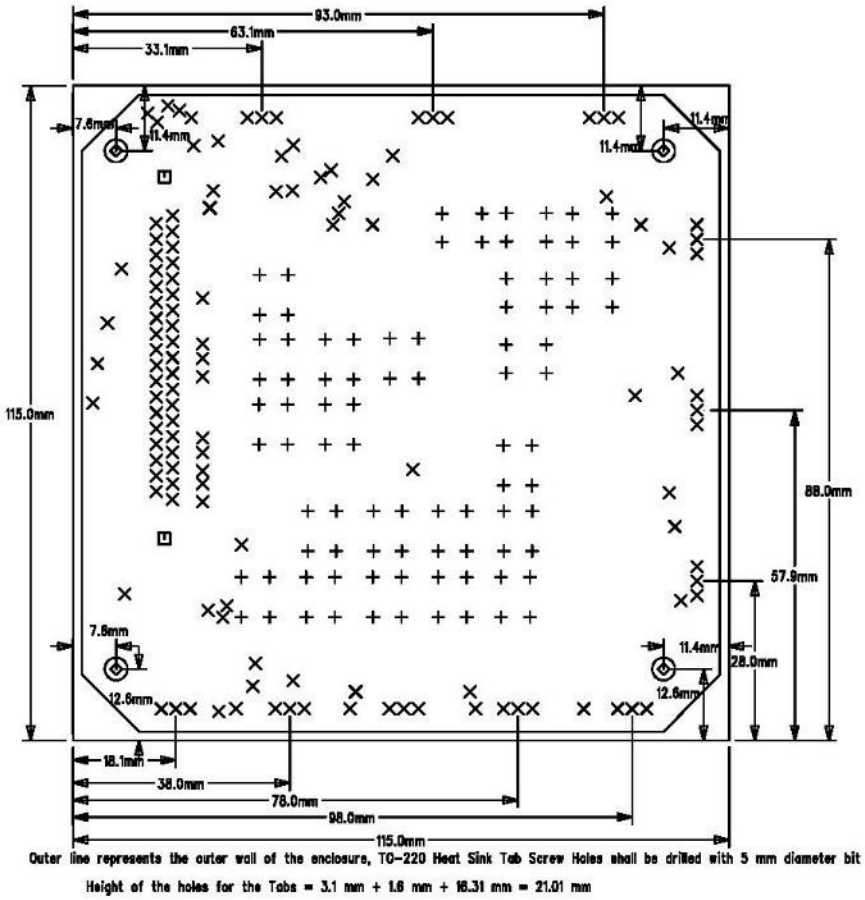


Figure E. 7 Miniature Semiconductor Measurement Board Assembly diagram



SIZE	QTY	SYM	PLATED	TOL
1.6	88	+	NO	+/-0.0
1	128	×	YES	+/-0.0
3.2	2	□	YES	+/-0.0
4	4	◇	YES	+/-0.0

Figure E. 8 Miniature Semiconductor Measurement Board initial Drill diagram. After the assembly of the board instead of drilling the heat tab holes transistors were clamped to the enclosure walls with mounting brackets using anodized aluminum heat sinks as insulation

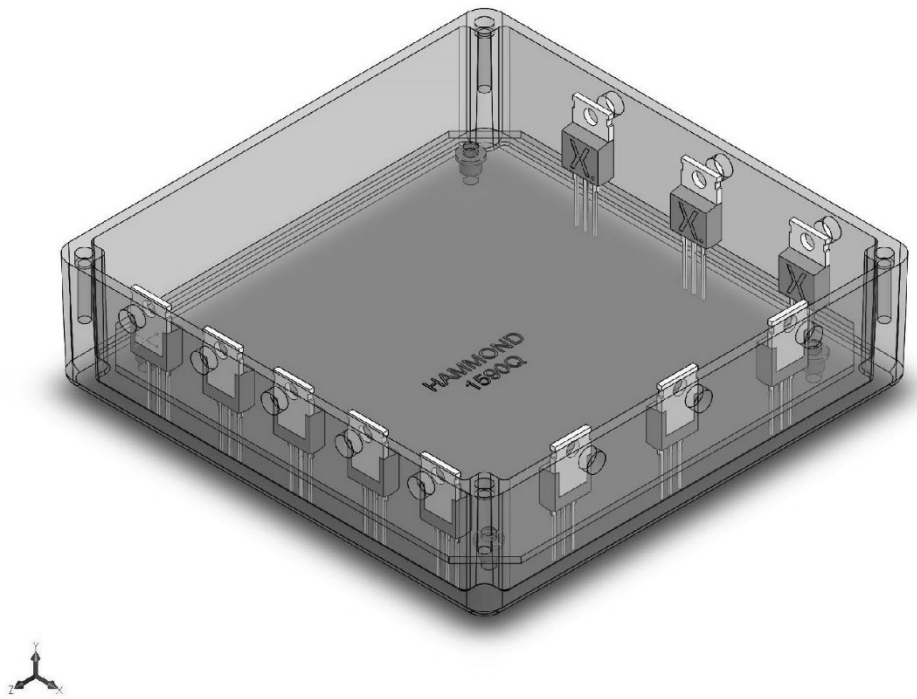


Figure E. 9 Initial Miniature Semiconductor Measurement Board 3D model. TO-220 package model was created by Nexperia**.** Enclosure model was created by Hammond. Spacer model was created by Würth Elektronic.

Sources for the ready-made 3D models:

- Nexperia, TO-220AB (SOT78), 3D model [WWW] https://www.nexperia.com/packages/SOT78.html)
- Hammond,1590WQBK, 3D model, [WWW] https://www.hammfg.com/part/1590WQBK
- Würth Electronik, WA-SMSR SMT Steel Spacer Reverse with internal Thread M 3, 3D model, [WWW] http://katalog.we-online.de/en/em/SMSR_SMD_STEEL_SPACER_M3_THREAD_INTERNAL

Table E. 1 Reference designators and descriptions of the components used in Miniature Semiconductor Measurement Board.

Item	Qty	Ref-Des	Part Name	Desc
1	22	J2-23	7767	4 Pin Screw Terminal, Power Tap M4 Through Hole
2	5	D1-5	FERD30M45CT	Standard Recovery Diode, 45 V, 30 A, Dual Common Cathode, 470 mV, 250 A
3	3	U1-3	IRF610PBF	MOSFET Transistor, N Channel, 3.3 A, 200 V, 1.5 ohm, 10 V, 4 V
4	3	U4-6	IRF9630PBF	MOSFET Transistor, P Channel, -6.5 A, -200 V, 800 mohm, -10 V, 4 V
5	8	J24-31	J601	Jumper (Busbar), Jumper, Single and Double Row Flat Mount Thermoset Terminal Blocks, 2 Ways
6	1	J1	L17HTNCHSOL2RM81C	D Sub Connector, 37 Contacts, Receptacle, DC, HTN Series, Steel Body, Through Hole
NON PCB				
2101-0180-04				Cable side D37 plug
9775031360R				Standoff, SMT, Steel, M3, Round Female, 3,1 mm, WA-SMSR Series
ÖLFLEX HEAT 180 0.50mm^2				Used as high current path in series connections

APPENDIX F: MINIATURE SEMICONDUCTOR BREAKOUT BOX

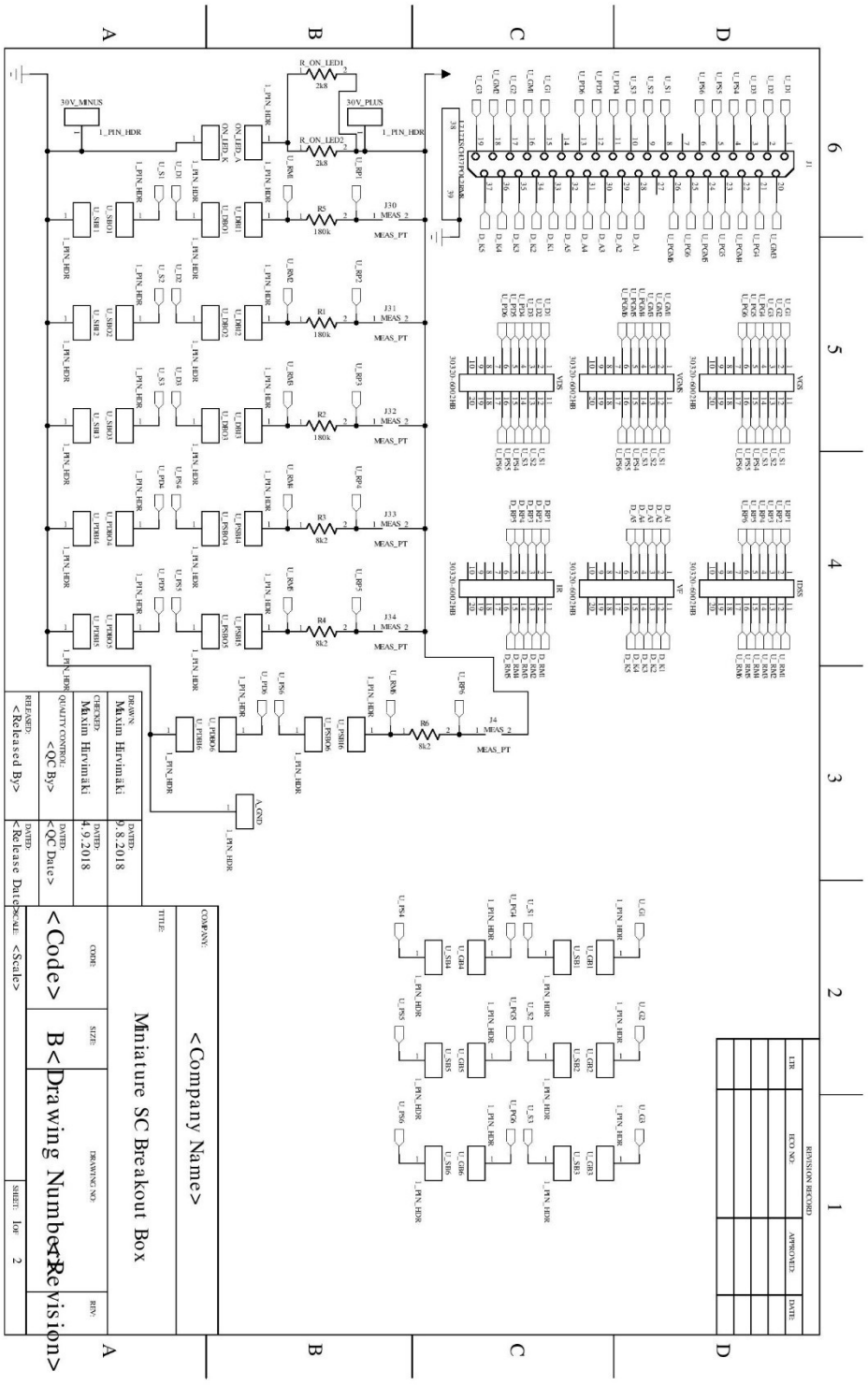


Figure F. 1 Miniature Semiconductor Breakout Box Schematic page 1

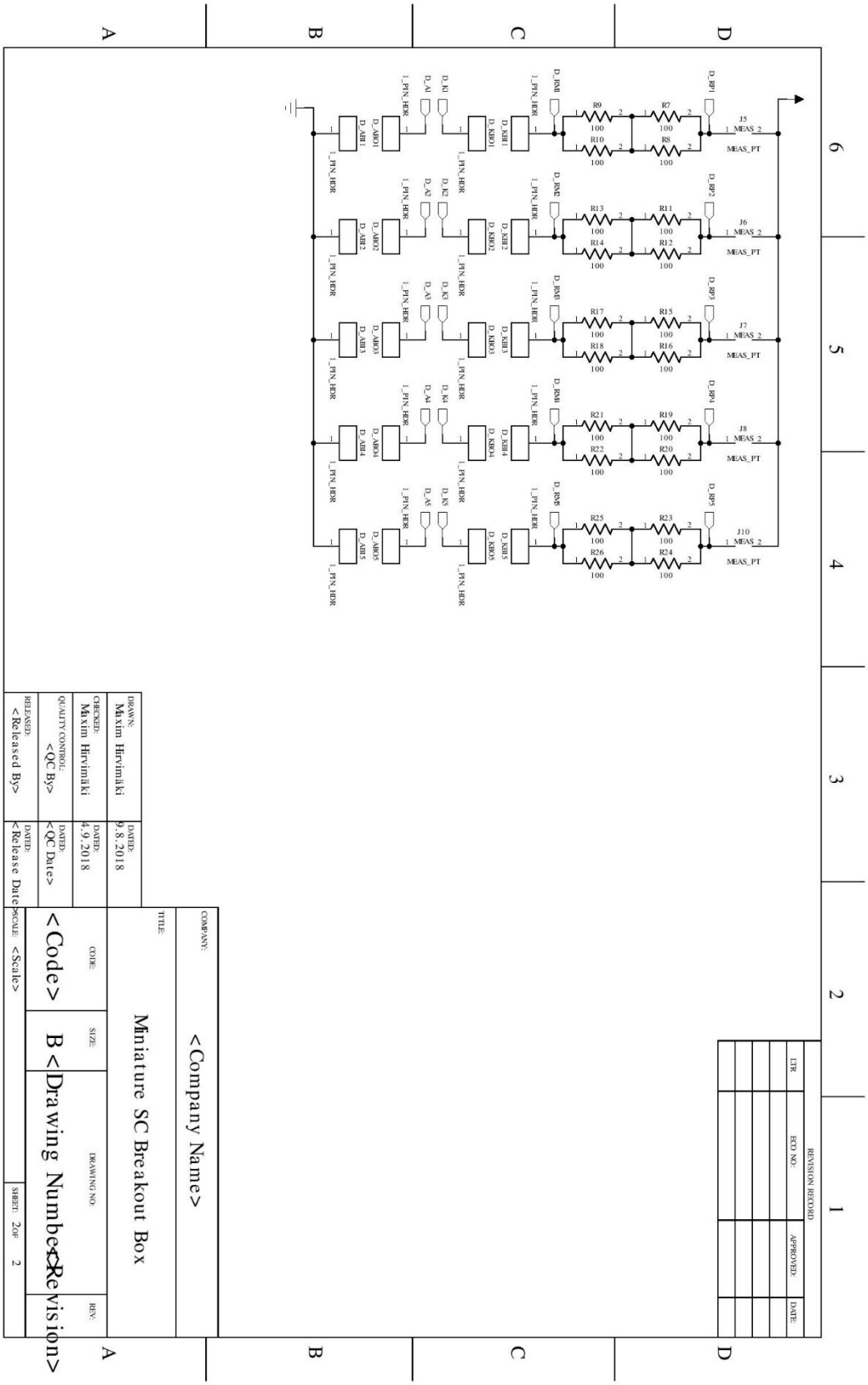


Figure F. 2 Miniature Semiconductor Breakout Box Schematic page 2

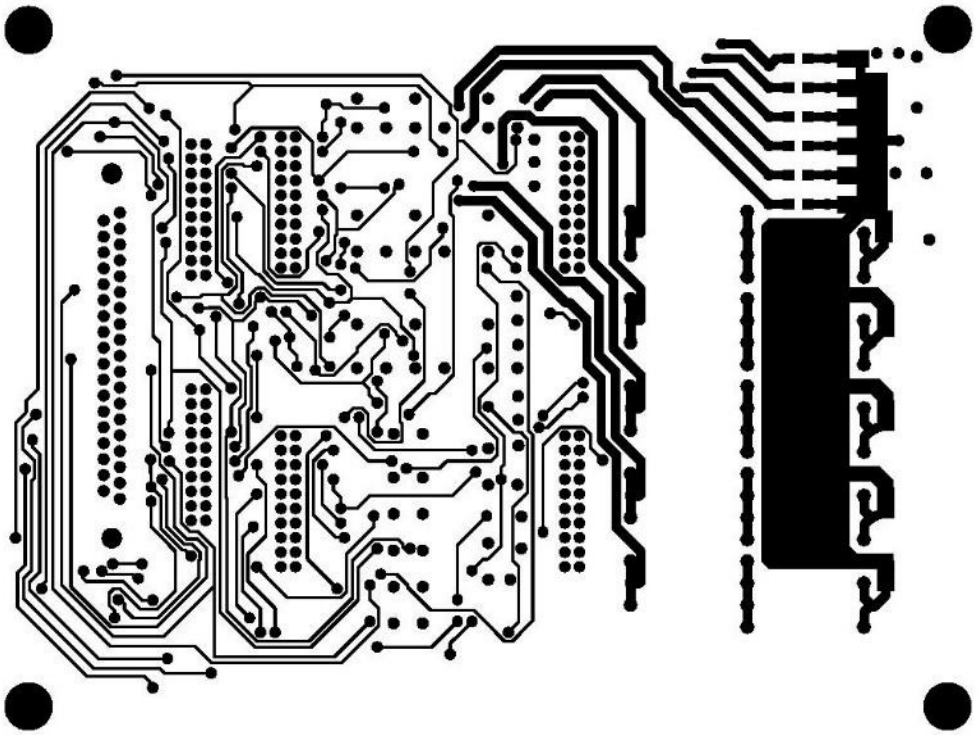


Figure F. 3 Miniature Semiconductor Breakout Box PCB Mask Top

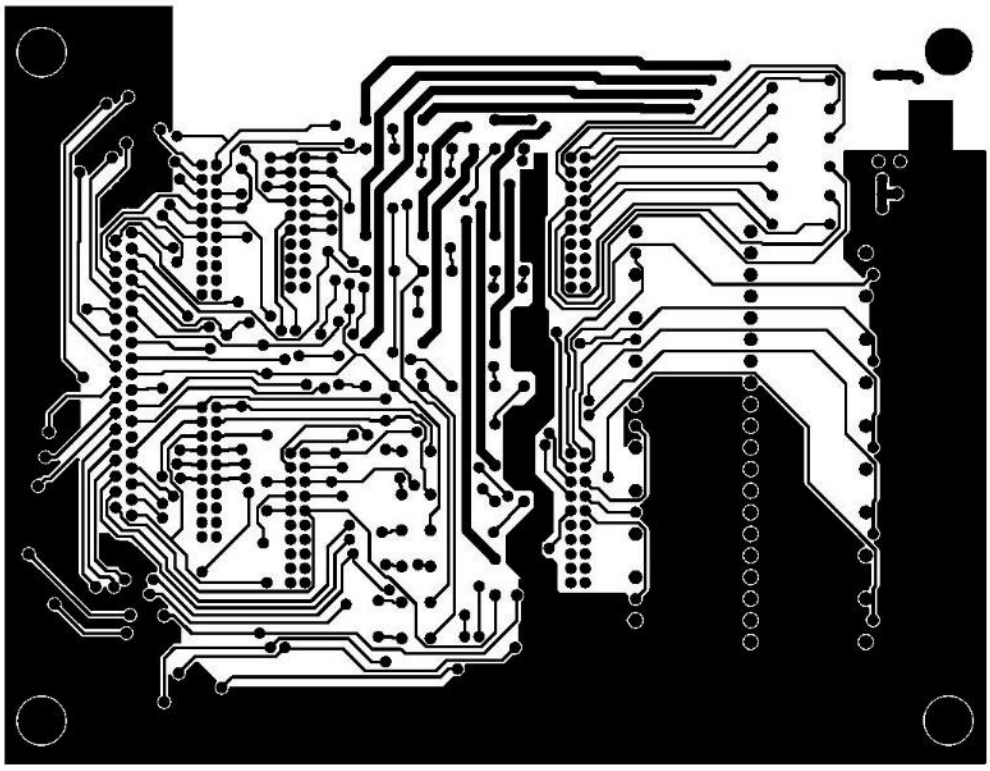


Figure F. 4 Miniature Semiconductor Breakout Box PCB Mask Bottom

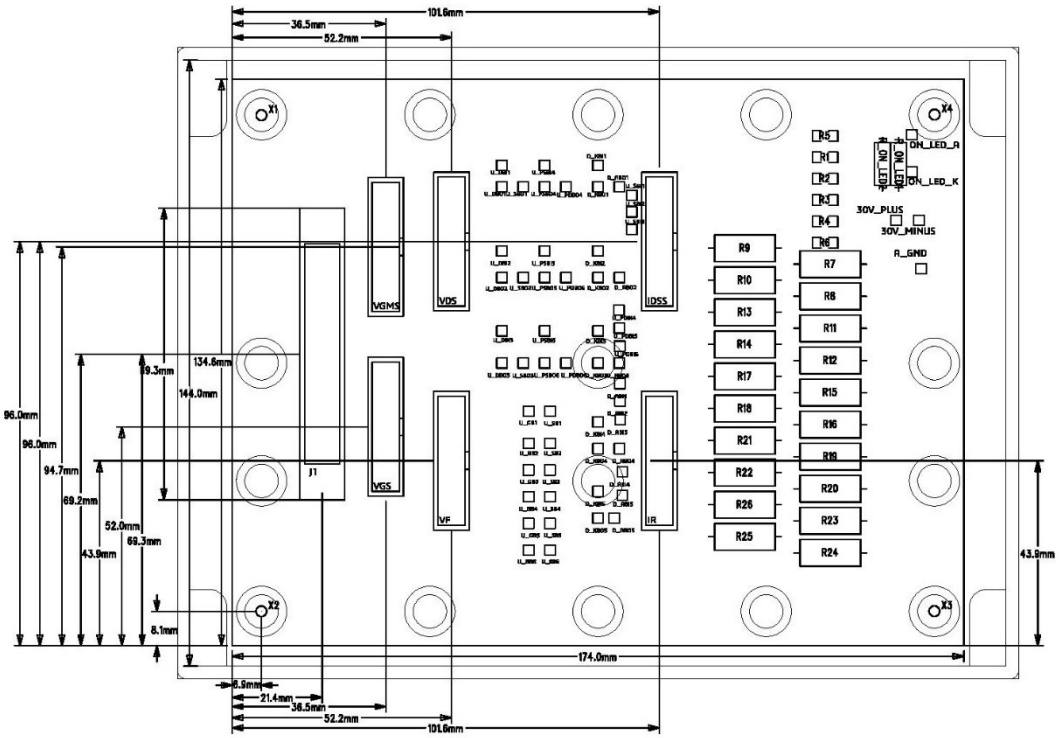
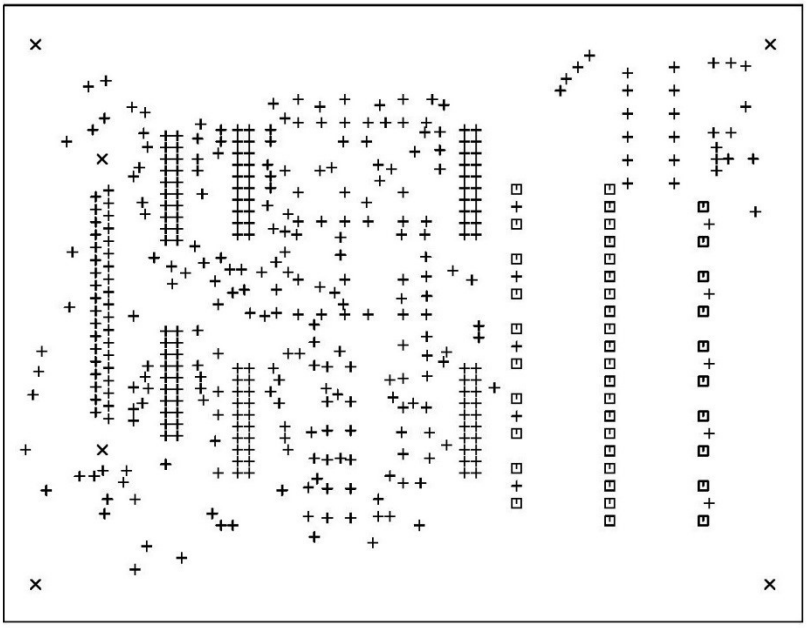


Figure F. 5 Miniature Semiconductor Breakout Box Assembly diagram. PCB size 175 mm x 145 mm



SIZE	QTY	SYM	PLATED	TOL
1	411	+	YES	+/-0.0
3	6	×	YES	+/-0.0
1.5	40	□	YES	+/-0.0

Figure F. 6 Miniature Semiconductor Breakout Box Drill diagram.

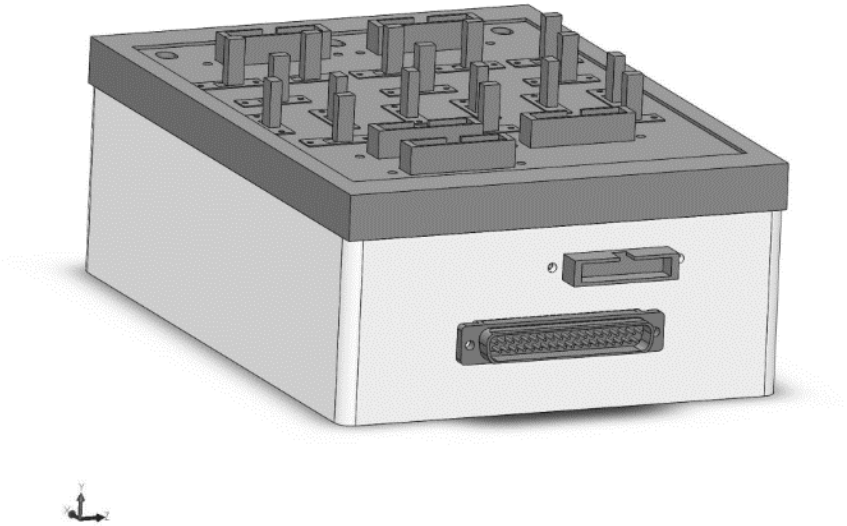


Figure F. 7 Miniature Semiconductor Breakout Box 3D model. 37 pin IDC connector model was created by TE Connectivity (TE Connectivity, 1658615-1 - D Sub Connector, 37 Contacts, Plug, DC, Amplimite HDF-20 Series, Plastic Body, IDC / IDT, 3D-model,[WWW] https://fi.farnell.com/amp-te-connectivity/1658615-1/plug-idc-d-plastic-37way/dp/1098384)

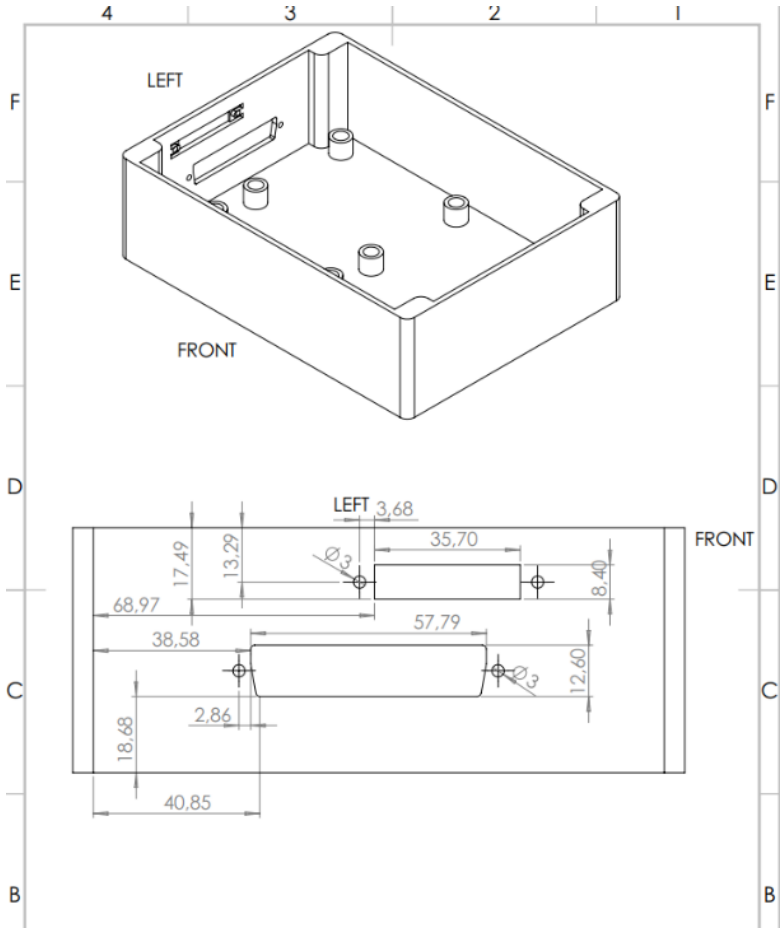


Figure F. 8 Miniature Semiconductor Breakout Box wall cutout. Dimensions in mm.

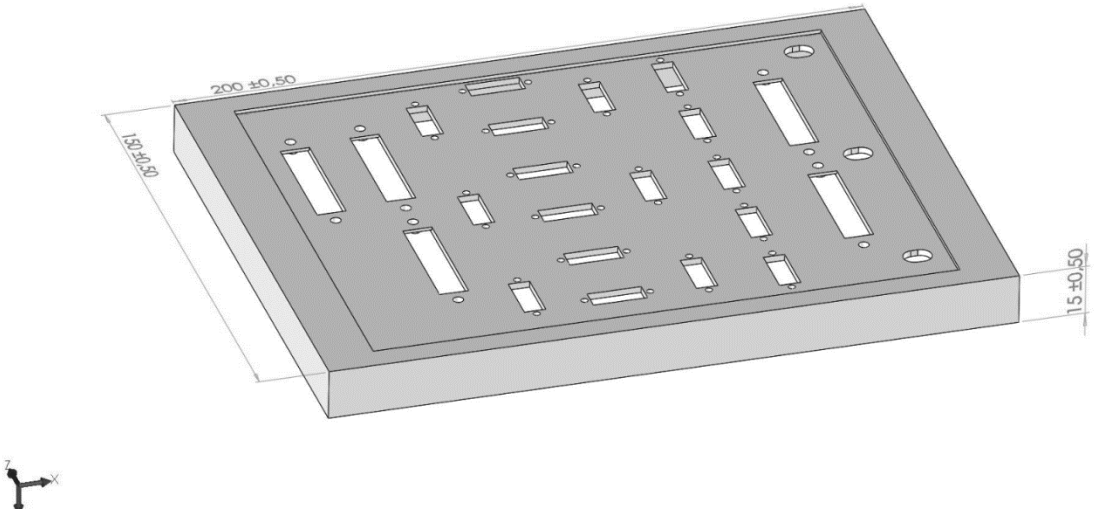


Figure F. 9 Miniature Semiconductor Breakout Box Lid 3D model initially used for printing. Indent on top of the lid was removed due to the printing process initially failing. Four 4 mm holes for lid mounting were drilled in the corners of the lid. One 4 mm hole was drilled in the lid for an indicator led.

Table F. 1 Reference designators and descriptions of the components used in Miniature Semiconductor Breakout Box

Item	Qty	Ref-Des	Part Name	Desc
1	11	J4-8,J10,J30-34		Separate path for measurements
2	20	R7-26		Through Hole Resistor, 100 ohm, MOR Series, 3 W, ± 5%, Axial Leaded, 350 V
3	61	30V_MINUS,30V_PLUS,A_GND,D_ABI1-5,D_ABO1-5,D_KBI1-5,D_KBO1-5,ON_LED_A,ON_LED_K,U_DBI1-3,U_DBO1-3,U_GB1-6,U_PDBI4-6,U_PDBO4-6,U_PSBI4-6,U_PSBO4-6,U_SB1-6,U_SBI1-3,U_SBO1-3	1 Pin Header	1 Position HEADER Connector Through Hole Tin
4	3	R1-2,R5	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 180k, 1/8W
5	3	R4,R3,R6	1206 Resistor	Surface Mount Resistorr, 1206 [3216 Metric], 8k2, 1/8W
6	6	J2-3,J9,J19,J24,J26	30320-6002HB	Wire-To-Board Connector, Four Wall, 2.54 mm, 20 Contacts,

				Header, 303 Series, Through Hole, 2 Rows
7	1	J1	L717TSCH37POL2RM8	D Sub Connector, 37 Contacts, Plug, DC, TS Series, Steel Body, Through Hole
8	1	R_ON_LED	MRS25000C1401FCT00	VISHAY Through Hole Resistor, 2,8 kohm, MRS25 Series, 600 mW, ± 1%, Axial Leaded, 350 V

NON-PCB

Part Name	Qty	Description
108-0903-001	2	JOHNSON - CINCH CONNECTIVITY Banana Test Connector, 4mm, Jack, Panel Mount, 15 A, 7 kV, Tin Plated Contacts, Black
108-0906-001	1	JOHNSON - CINCH CONNECTIVITY Banana Test Connector, Jack, Panel Mount, 15 A, 7 kV, Tin Plated Contacts, Orange
9-1437356-1	6 x 20 cm	TE CONNECTIVITY Ribbon Cable, Flat, 20 Core, 28 AWG, 0,072 mm², Blue
SLIDE SWITCH MINIATURE DPCO	17	MULTICOMP Slide Switch, DPDT, Panel, 500 mA
76347-302LF	61	AMPHENOL ICC (FCI) Contact, DUBOX Basics+ Series, Socket, Crimp, 22 AWG, Gold Plated Contacts
D89120-0131HK	6	3M Wire-To-Board Connector, 2,54 mm, 20 Contacts, Receptacle, D89 Series, IDC / IDT, 2 Rows
R2651DTSY40SC85	5 cm (3 cores removed)	PRO POWER Ribbon Cable, Per Meter, 40 Core, 28 AWG, Grey
5501-37SA-02-F1	1	MULTICOMP D Sub Connector, 37 Contacts, Receptacle, DC, D Sub, Solder
8FSM37P-30N1-FEC	2	MULTICOMP D Sub Connector, 37 Contacts, Plug, DC, Metal D Series, Metal Body, IDC / IDT
354-311-04	1	MARL LED Panel Mount Indicator, Yellow, 2 VDC, 4,1 mm, 20 mA, 20 mcd, Not Rated

APPENDIX G: MINIATURE MOSFET GATE CONTROL BOARD

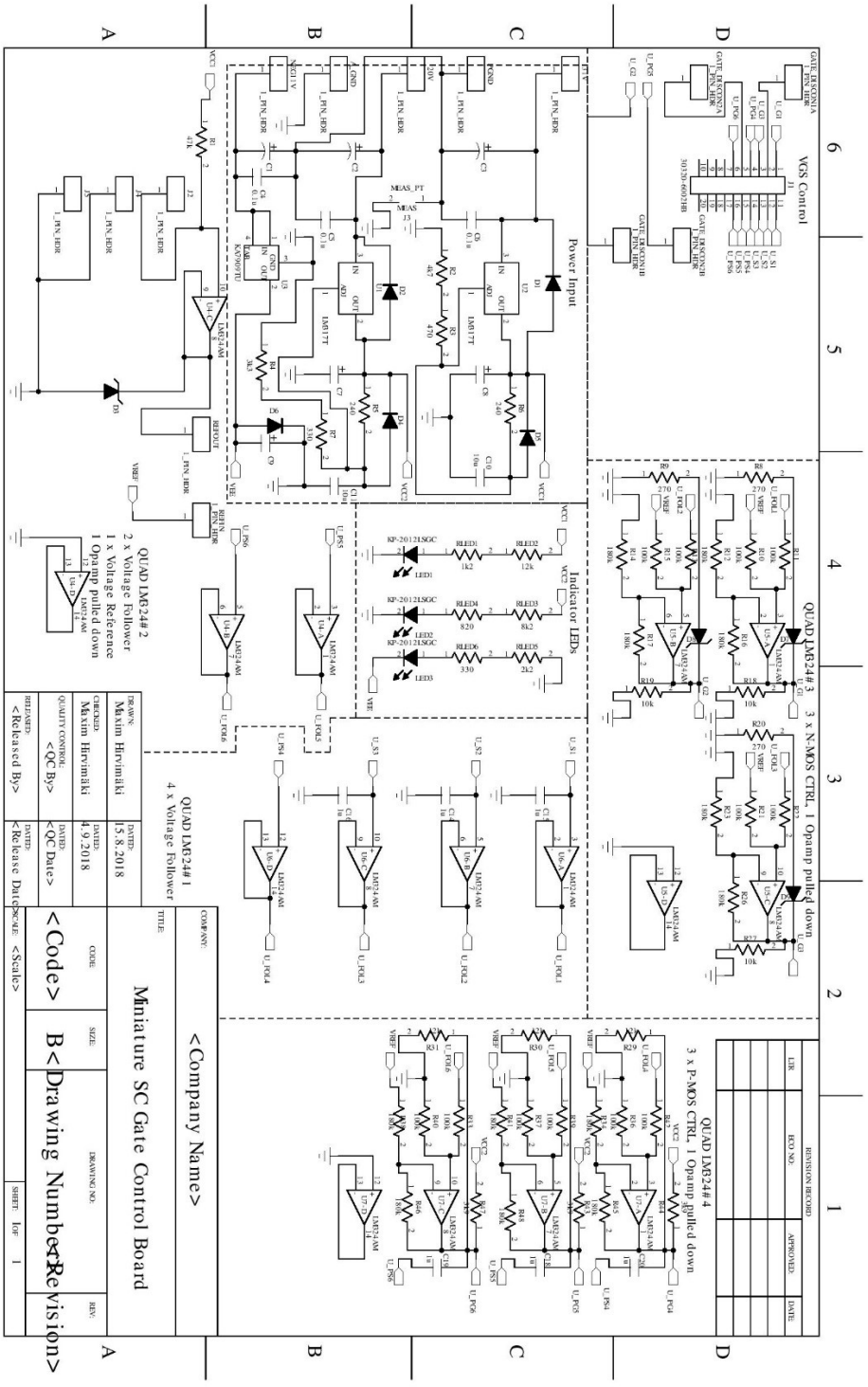


Figure G. 1 Miniature MOSFET Gate Control Board Schematic

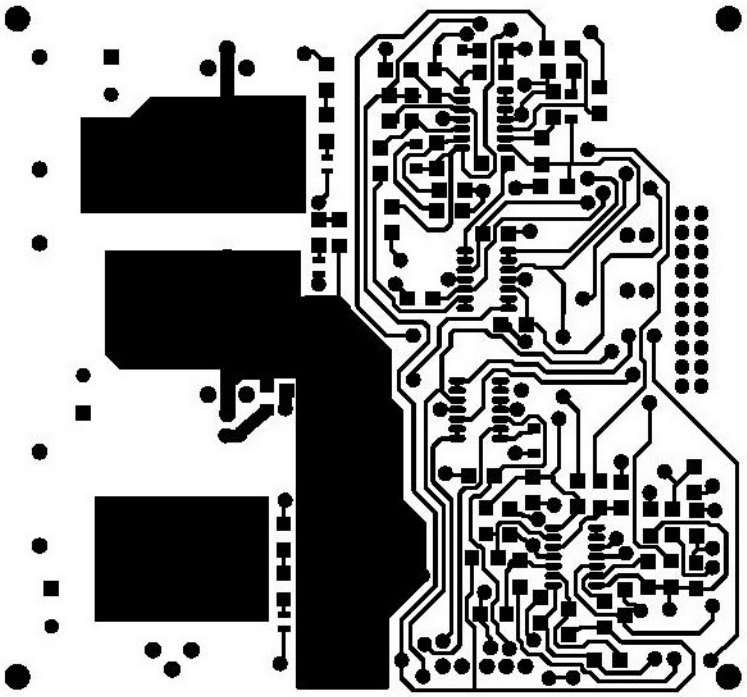


Figure G. 2 Miniature MOSFET Gate Control Board PCB Mask Top

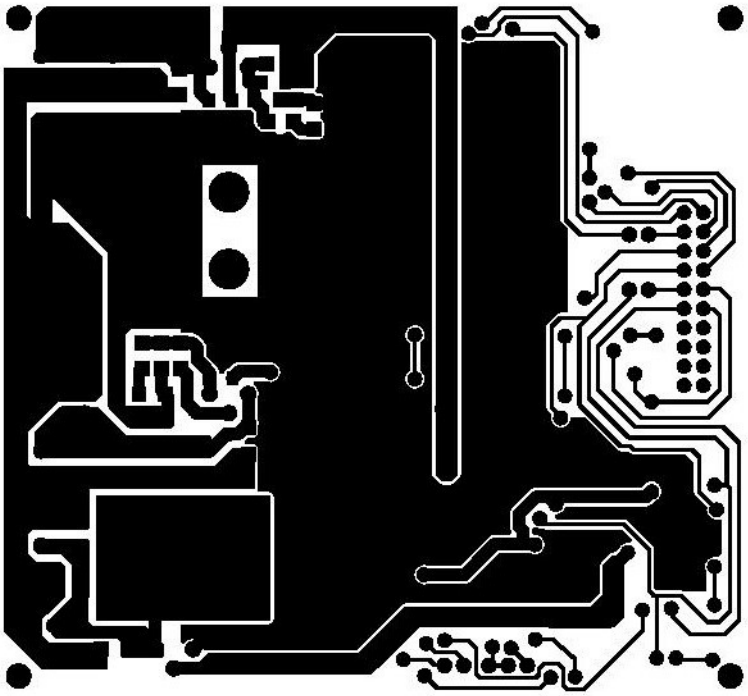


Figure G. 3 Miniature MOSFET Gate Control Board PCB Mask Bottom

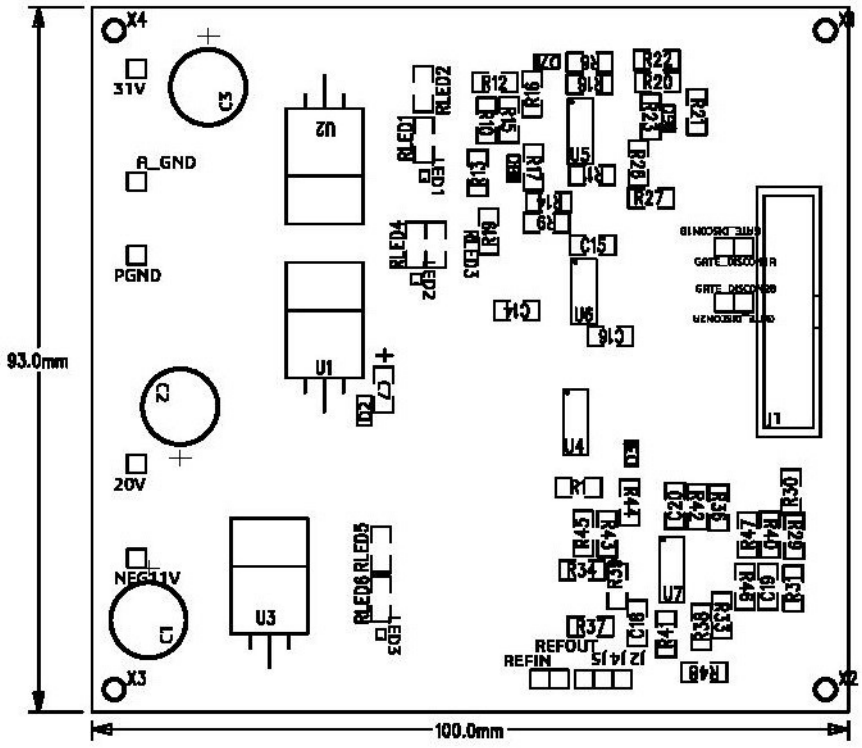


Figure G. 4 Miniature MOSFET Gate Control Board Assembly diagram Top. PCB size 95 mm x 100 mm

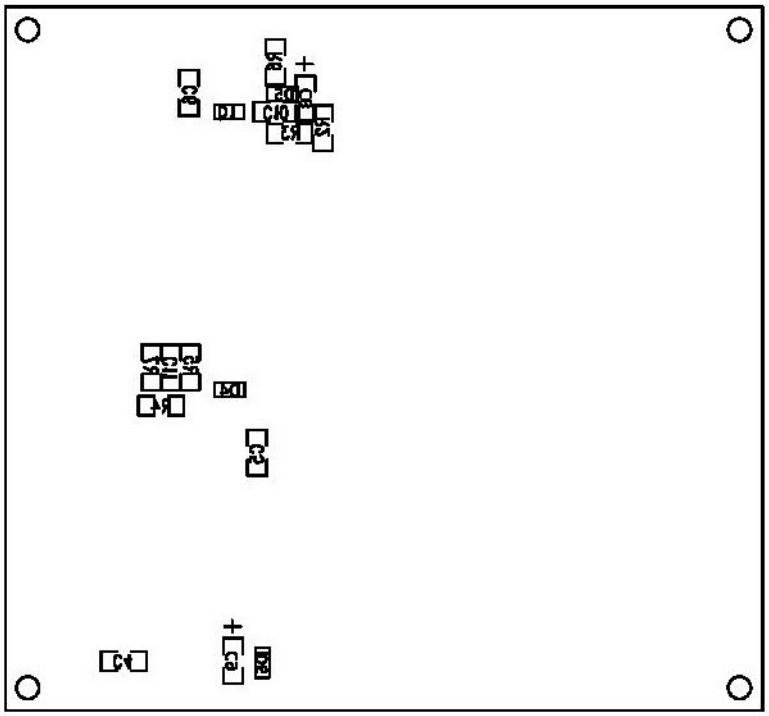
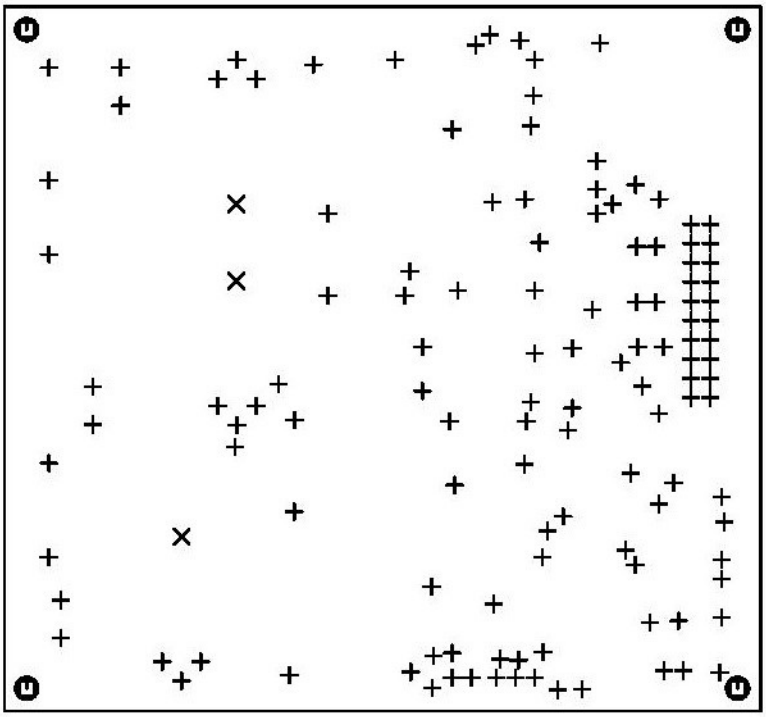


Figure G. 5 Miniature MOSFET Gate Control Board Assembly diagram Bottom.



SIZE	QTY	SYM	PLATED	TOL
1	125	+	YES	+/-0.0
4	3	×	YES	+/-0.0
3	4	⊡	YES	+/-0.0

Figure G. 6 Miniature MOSFET Gate Control Board Drill diagram.

Table G. 1 Reference designators and descriptions of the components used in MOSFET Gate Control Board

Item	Qty	Ref-Des	Part Name	Desc
1	1	U3	KA7909TU	Linear Voltage Regulator, 7909, Fixed, -35V To -10V In, -9V And 1A Out, TO-220AB-3
2	2	U1-2	LM317	POSITIVE VOLTAGE REGULATOR; ADJUSTABLE
3	4	U4-7	LM324	QUAD,LOW POWER OP AMP
4	2	R5-6	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 240, 1/8W
5	3	R8-9,R20	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 270, 1/8W
6	14	20V,31V,A_GND,GATE_DISCON1A,GATE_DISCON1B,GATE_DISCON2A,GATE_DISCON2B,J2,J4-5,NEG11V,PGND,REFIN,REFOUT	1 Pin Header	1 Position HEADER Connector Through Hole Tin
7	2	C10-11	1206 Ceramic Capacitor	Surface Mount Ceramic Capacitor, 1206 [3216 Metric], 10u,50V
8	6	C14-16,C18-20	1206 Ceramic Capacitor	Surface Mount Ceramic Capacitor, 1206 [3216 Metric], 1u,50V
9	1	R1	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 47k, 1/8W
10	1	R2	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 4.7k, 1/8W
11	1	R3	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 470, 1/8W
12	1	R4	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 3.3k, 1/8W
13	2	R7,RLED6	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 330, 1/8W
14	12	R11,R13,R15,R21-22,R33,R36-37,R39-40,R42,R10	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 100k, 1/8W
15	6	R26,R16-17,R14,R12,R23	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 180k, 1/8W
16	6	R34,R38,R41,R45-46,R48	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric],180k, 1/8W
17	3	R18-19,R27	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 10k, 1/8W
18	3	R44,R47,R43	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 3k9, 1/8W
19	4	R29-30,RLED2,R31	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 12k, 1/8W
20	1	RLED3	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 8.2k, 1/8W
21	1	RLED4	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 820, 1/8W
22	1	RLED5	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 2.2k, 1/8W
23	1	RLED1	1206 Resistor	Surface Mount Resistor, 1206 [3216 Metric], 1.2k, 1/8W
24	1	C9	1206 Tantalum	Surface Mount Tantalum Capacitor, 1206 [3216 Metric],1u,50V
25	1	C7	1206 Tantalum Capacitor	Surface Mount Tantalum Capacitor, 1206 [3216 Metric], 1u, 50V
26	1	C8	1206 Tantalum Capacitor	Surface Mount Tantalum Capacitor, 1206 [3216 Metric], 1u, 50V
27	1	J1	30320-6002HB	Wire-To-Board Connector, Four Wall, 2.54 mm, 20 Contacts, Header, 303 Series, Through Hole, 2 Rows
28	1	J6	504222B00000G	Heat Sink, Square, PCB, 6.4 °C/W, TO-220, 19.81 mm, 21.59 mm, 36.83 mm
29	1	C2	Electrolytic Capacitor Can	Electrolytic Capacitor, 100u, 50V
30	3	C4-6	Ceramic Capacitor 1206	Surface Mount Ceramic Capacitor, 1206 [3216 Metric], 0.1u,50V

31	1	C1	Electrolytic Capacitor, 100u, 50V	100µF 50V Aluminum Electrolytic Capacitors Radial, Can
32	1	C3	Electrolytic Capacitor, 330u, 50V	330µF 50V Aluminum Electrolytic Capacitors Radial, Can
33	3	LED1-3	KP-2012LSGC	LED, Low Power, Green, SMD, 2 mA, 1.9 V, 568 nm
34	4	D3,D7-9	MMSZ5243B-TP	Zener Diode 13V 500mW ±5% Surface Mount SOD-123
35	5	D1-2,D4-6	S1AL	Standard Recovery Diode, Glass Passivated, 50 V, 1 A, Single, 1.1 V, 1.8 µs, 30 A

NON-PCB

Part Name	Qty	Desc
9-1437356-1	50cm	TE CONNECTIVITY Ribbon Cable, Flat, 20 Core, 28 AWG, 0,072 mm², Blue
R16148-1B-1-A50K	1	Potentiometer: shaft; single turn; 50kΩ; 63mW; ±20%; on cable; 6mm
76347-302LF	8	AMPHENOL ICC (FCI) Contact, DUBOX Basics+ Series, Socket, Crimp, 22 AWG, Gold Plated Contacts
2.54 mm Jumper	6	Shorting jumper with 2.54 mm pitch
22,5068 + 22,2060-24	5	STAUBLI,STAUBLI Banana Test Connector, 4mm, Plug, Cable Mount, 20 A, 60 V, Nickel Plated Contacts, Yellow

APPENDIX H: OSCILLOSCOPE CHANNEL SELECTOR

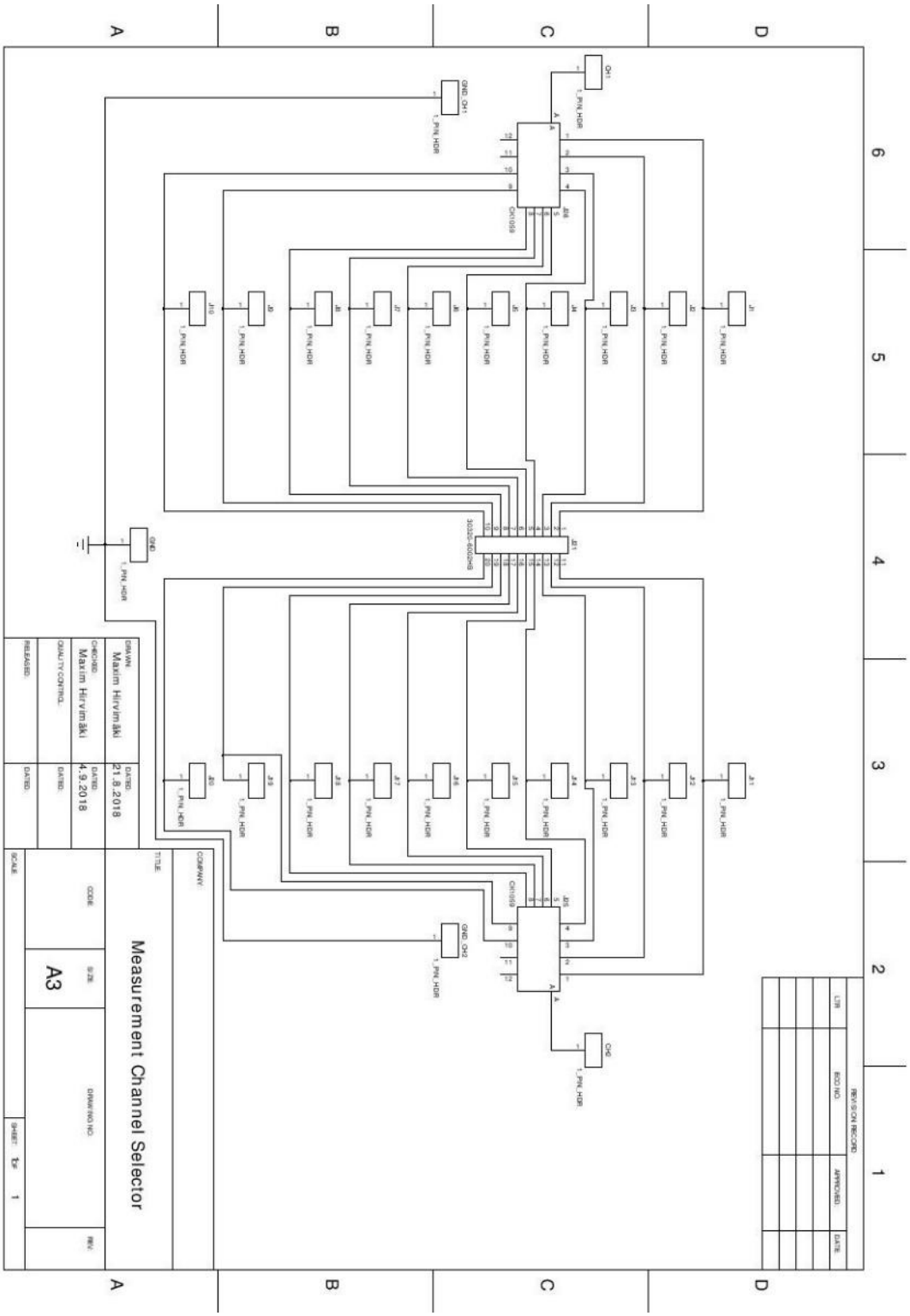


Figure H. 1 Oscilloscope Channel Selector Schematic

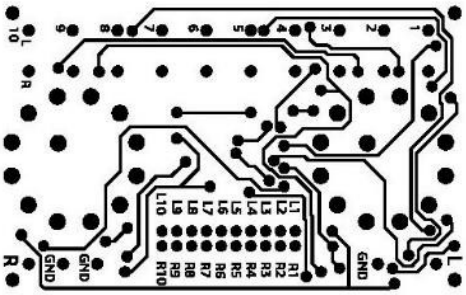


Figure H. 2 Oscilloscope Channel Selector PCB Mask Top

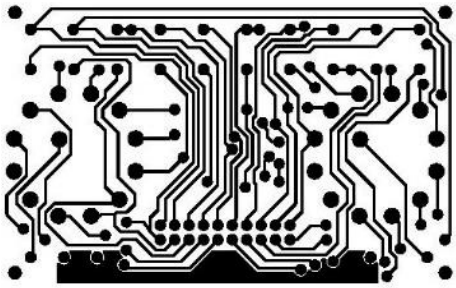


Figure H. 3 Oscilloscope Channel Selector PCB Mask Bottom

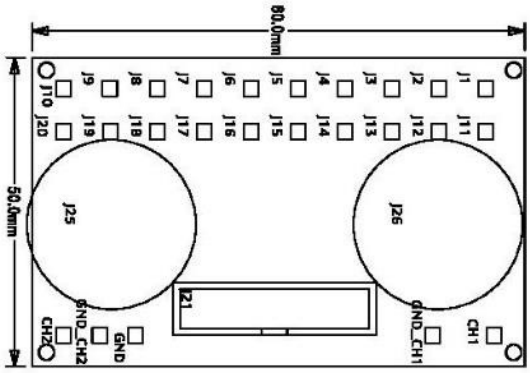


Figure H. 4 Oscilloscope Channel Selector Assembly diagram. PCB size 50 mm x 80 mm

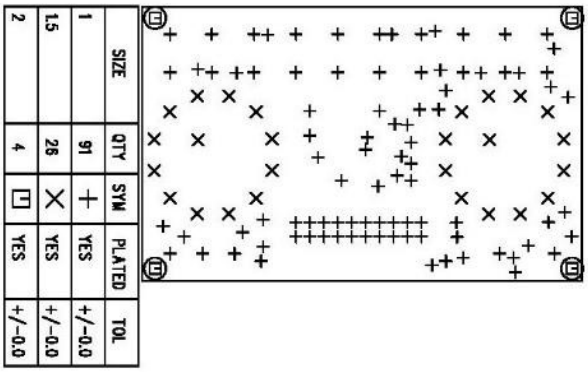


Figure H. 5 Channel Selector Drill diagram

Table H. 1 Reference designators and descriptions of the components used in Oscilloscope Channel Selector

Item	Qty	Ref-Des	Part Name	Desc
1	2	J25-26	CK1059	LORLIN Rotary Switch, 12 Position, 1 Pole, 30 °, 150 mA, 250 V, CK Series
2	25	CH1-2,GND,GND_CH1-2,J1-20	1 Pin Header	1 Position HEADER Connector Through Hole Tin
3	1	J21	30320-6002HB	Wire-To-Board Connector, Four Wall, 2.54 mm, 20 Contacts, Header, 303 Series, Through Hole, 2 Rows

APPENDIX I: THRESHOLD VOLTAGE WAVEFORMS

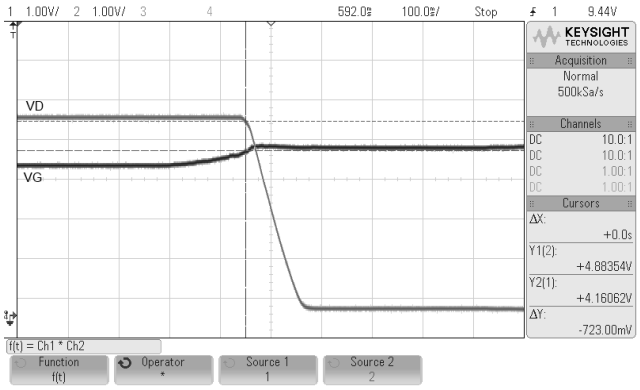


Figure I. 1 VGSTH measurement of transistor U1

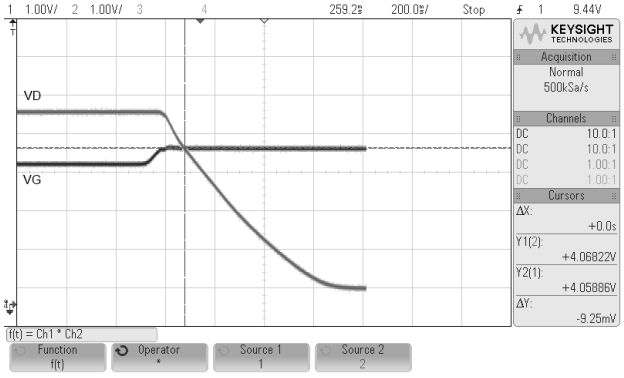


Figure I. 2 VGSTH measurement of transistor U2

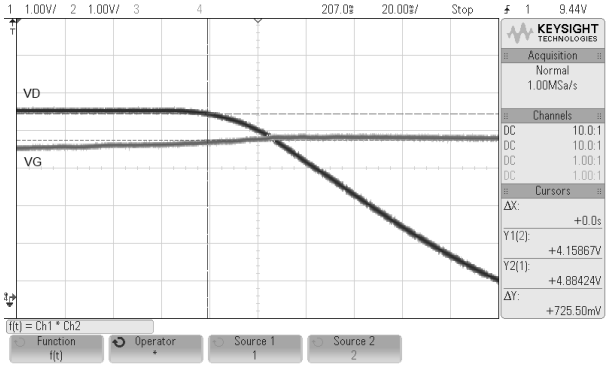


Figure I. 3 VGSTH measurement of transistor U3

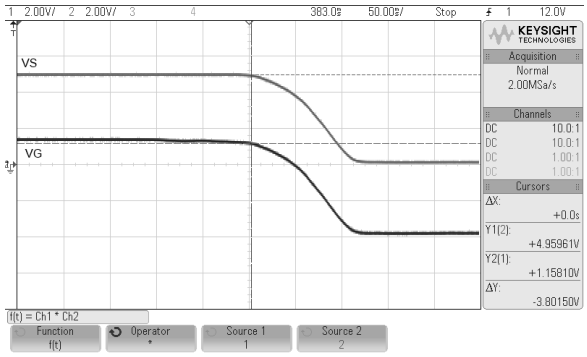


Figure I. 4 VGSTH measurement of transistor U4

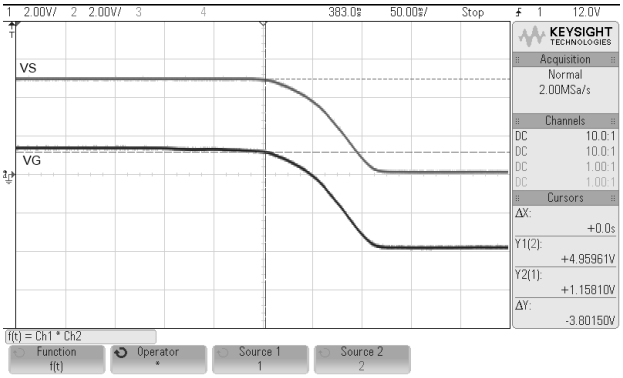


Figure I. 5 VGSTH measurement of transistor U5

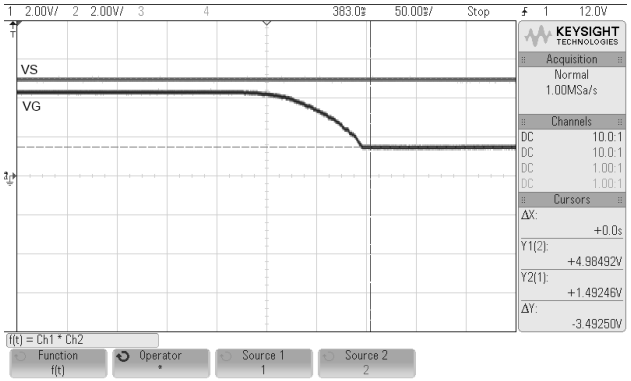


Figure I. 6 Failure to reach the threshold voltage of transistor U6 due to the damaged output on the MOSFET Gate Control Board

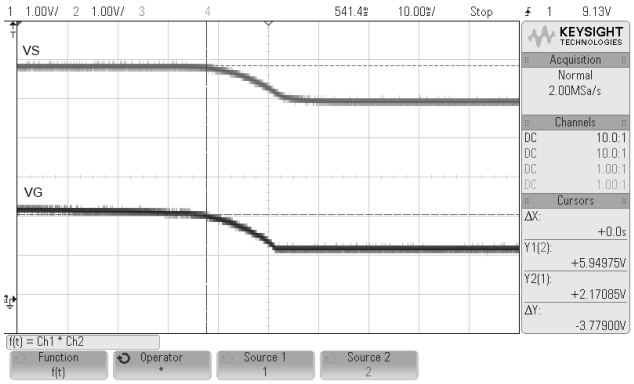


Figure I. 7 VGSTH measurement of transistor U6 after Source-to-Drain test voltage was changed to 6 V.

APPENDIX J: MOSFET SERIES CONNECTION WAVEFORMS WITHOUT VOLTAGE FOLLOWER CAPACITORS

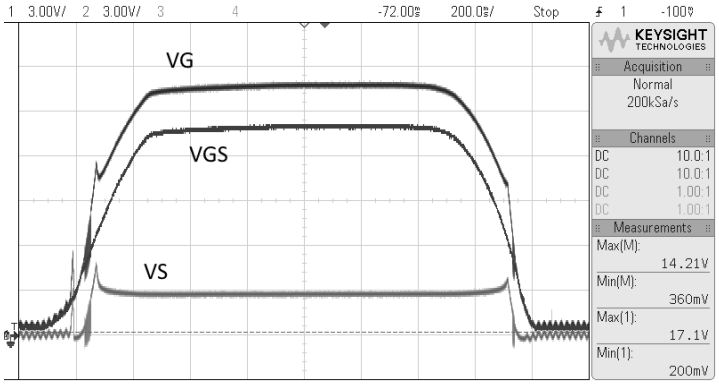


Figure J. 1 V_{GS} waveform of transistor U1 without input capacitors on the voltage followers.

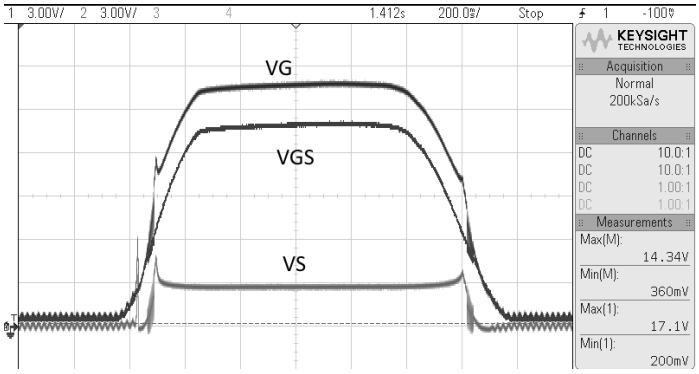


Figure J. 2 V_{GS} waveform of transistor U2 without input capacitors on the voltage followers.

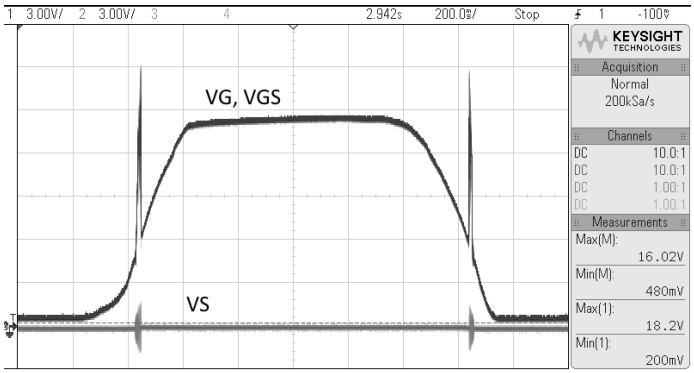


Figure J. 3 VGS waveform of transistor U3 without input capacitors on the voltage followers. VGS spikes over 16 V

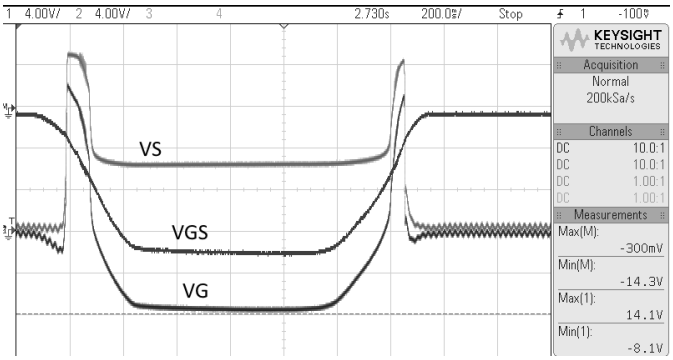


Figure J. 4 VGS waveform of transistor U4 without input capacitors on the voltage followers.

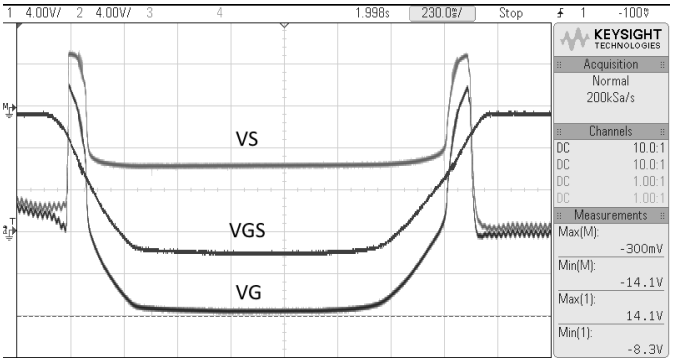


Figure J. 5 VGS waveform of transistor U5 without input capacitors on the voltage followers.

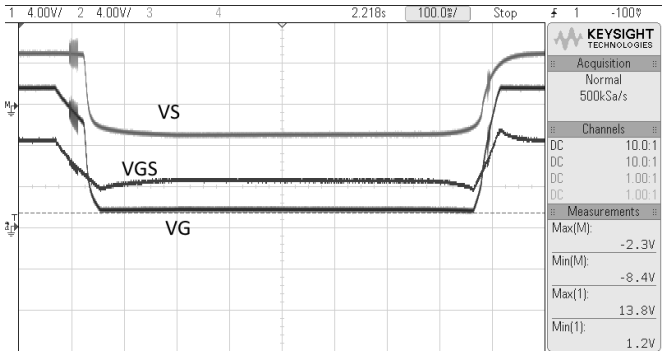


Figure J. 6 VGS waveform of transistor U6 without input capacitors on the voltage followers.